SCT3604 Datasheet

Broadband High Efficient RF Power Amplifier

V. 1.0 Nov, 2011

CONTENTS

| 1. | PRODUCT INTRODUCTION | 3 |
|-----|----------------------------|----|
| 2. | FEATURES | 3 |
| 3. | TYPICAL APPLICATIONS | 3 |
| 4. | ABSOLUTE MAXIMUM RATINGS | 4 |
| 5. | ELECTRICAL CHARACTERISTICS | 4 |
| 6. | BLOCK DIAGRAM | 6 |
| 7. | PIN DESCRIPTION | 7 |
| 8. | APPLICATION INFORMATION | 8 |
| 9. | TEST SCHEMATIC AND LAYOUT | 9 |
| 10. | MAIN CHARACTERISTICS | 10 |
| 11. | PACKAGING INFORMATION | 11 |
| 12. | DISCLAIMERS | 12 |
| | | |

1. PRODUCT INTRODUCTION

SCT3604 is a high-gain and high-efficiency power amplifier chip offering high performance and wideband in CW or FM signal amplifications, especially for VHF, UHF Walkie-Talkie, RFID and other FM, FSK, ASK applications in a frequency range from 130MHz to 1GHz. The chip is fabricated on silicon process. Its input and output matches are implemented on printed circuit board and can be easily adjusted to obtain optimum power and efficiency. The chip is assembled in a low thermal resistance 5x5 mm² QFN28 package.

2. FEATURES

- Single supply voltage from 2.5 to 6 V
- Wide operation frequency range from 130 MHz to 1 GHz
- High power gain up to 38 dB
- High output power up to 34 dBm at 4.2 V
- High power added efficiency of 55%
- 5x5 mm² plastic QFN28 in 0.5mm pitch

3. TYPICAL APPLICATIONS

- Analog walkie-talkies, like Family Radio Service (FRS), General Mobile Radio Service (GMRS)
- Digital FDMA two way radio and trunking systems (DPMR, P25, DCR, NXDN, NDR)
- Digital TDMA two way radio and trunking systems (DMR, P25, PDT)
- Wireless data communication (FSK, AFSK, OOK, GFSK, MSK)
- RFID reader/writers
- Wireless sensor network and AdHoc application
- Remote control and sensing systems
- Commercial and consumer electronics
- Portable and battery powered equipments

4. ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings given in table must not be violated under any circumstances. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

| Parameter | Specification | | Unit | Condition | |
|------------------------|---------------|------|------|-----------|--|
| | Min | Тур. | Max | | |
| Supply voltage | -0.5 | | 12.0 | V | |
| Voltage per pin | -0.5 | | 12.0 | V | |
| Current per pin | -0.5 | | 0.5 | А | |
| RF Power per pin | | | 30 | dBm | |
| Output load VSWR | | | 20:1 | | |
| ESD protection voltage | 1.0 | | | kV | |
| Thermal resistance | | 10 | | °C /W | |
| Lead temperature | | | 260 | °C | |
| Storage temperature | -50 | | 150 | °C | |

5. ELECTRICAL CHARACTERISTICS

| Parameter | Specification | | Unit | Condition | |
|------------------------------|---------------|------|------|-----------|--|
| | Min | Тур. | Max | | |
| Supply voltage (VDD) | 2.5 | | 6 | V | In AC condition |
| Bias control voltage | 0.0 | | 2.0 | V | |
| DC supply current | | 1.2 | | А | <pre>@Pout = 34 dBm @VDD = 4.2V</pre> |
| Operation temperature | -40 | | 85 | °C | |
| Operating frequency range | 130 | | 1000 | MHz | |
| Maximum output power Pmax | | 34 | | dBm | $\begin{array}{l} @Pin = -5 \ dBm \\ @VDD = 4.2 \ V \end{array}$ |

4

| Power added efficiency (PAE) | 55 | 60 | % | @ Pout = 2.5W @ VDD = 4.2 V @ Freq = 150MHz |
|---------------------------------|------|-----|-----|---|
| Input power for Pmax | -5 | | dBm | |
| ACPR | | -70 | dBc | @1.0kHz narrow band FM signal |
| Forward isolation | 60 | | dB | |
| Second harmonic | -30 | | dBc | @ Pmax |
| Third harmonic | -45 | | dBc | @ Pmax |
| Fourth harmonic | -60 | | dBc | @ Pmax |
| Other non-harmonic spurious | | -60 | dBc | @ Pmax |
| Input VSWR | 2.0: | | | External matching to |
| | 1.0 | | | 50Ω source |
| Output load VSWR | 4.0: | | | External matching to |
| 1 | 1.0 | | | 50Ω load |



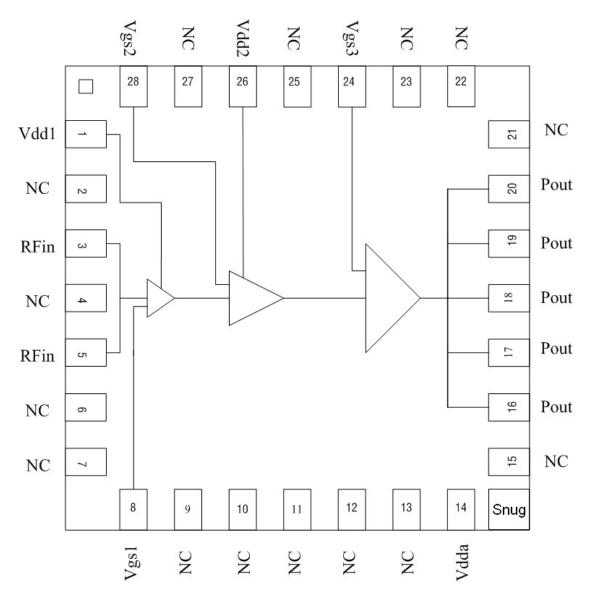


Fig.1. Block Diagram (5x5 mm² QFN28)

7. PIN DESCRIPTION

| Pin No. | Pin Name | Pin Type | Description | | | |
|---------|----------|-----------------|--|--|--|--|
| 1 | Vdd1 | Power supply | Power supply for first stage | | | |
| 2 | NC | - | No connection | | | |
| 3 | RFin | RF input | RF signal input and off chip DC blocking capacitor is required | | | |
| 4 | NC | - | No connection | | | |
| 5 | RFin | RF input | Same as Pin 2 | | | |
| 6 | NC | - | No connection | | | |
| 7 | NC | - | Grounding | | | |
| 8 | Vgs1 | Analog input | Bias input for first stage, (Ref. to application schematic for details) | | | |
| 9 | NC | - | No connection | | | |
| 10 | NC | - | No connection | | | |
| 11 | NC | - | No connection | | | |
| 12 | NC | - | No connection | | | |
| 13 | NC | - | No connection | | | |
| 14 | Vdda | Power supply | Power supply for analogy circuits | | | |
| 15 | NC | | No connection | | | |
| 16 | RFout | | Power supply and RF output for the | | | |
| 17 | RFout | | output stage. External matching is required to get maximum output power and PAE. (Ref. to application schematic for details.) | | | |
| 18 | RFout | - RF power | | | | |
| 19 | RFout | – output | | | | |
| 20 | RFout | | | | | |
| 21 | NC | - | No connection | | | |
| 22 | NC | - | No connection | | | |
| 23 | NC | - | No connection | | | |
| 24 | Vgs3 | Analog input | Bias input for output stage, (Ref. to application schematic for details.) | | | |
| 25 | NC - | | No connection | | | |
| 26 | Vdd2 | Power supply | Power supply for second stage. | | | |
| 27 | NC | - | No connection | | | |
| 28 | Vgs2 | Analog input | Bias input for second stage. (Ref. to application schematic for details.) | | | |
| Snug | GND | Ground | Grounding and thermal radiation | | | |

Pin out and their functions in the table below are defined for the chip SCT3604.

8. APPLICATION INFORMATION

SCT3604 is a three-stage power amplifier device with high gain at full output power. An input power of -5 dBm is required to achieve its fully saturate output power. The chip requires only a single positive power supply. The amplifier's main ground is the big and exposed pad in the middle of the package at the bottom (the snug as indicated on the chip symbol), and the pad should be connected to PCB ground plate with 20-25 vias for good thermal conductivity and grounding.

A special care must be taken care for the multi via layout of the PCB. The 10 mil hole size is recommended and the via must be from top layer to bottom layer. At the same time, an excellent thermal radiator or excellent thermal connection between the chip and the alloy frame of the system.

In normal application for signal with constant envelope, the first and second stages of the amplifier are in class-A and class-AB mode, respectively. The third stage of the amplifier operates in class-C mode. Its DC current will be increased with RF input signal. The optimum load for maximum output power and efficiency is approximately 5 Ω . An external output matching network is required to match this impedance to 50 Ω load, referring to the test and application schematic for more details. The chip inputs (pin 3 and 4) are DC biased, thus a blocking capacitor must be inserted in series between signal source and the chip inputs.

Vdd1 and Vdd2 provide DC power supply to the first and second stages, respectively. RF chock inductor is need for each pin. Vgs1, Vgs2 and Vgs3 should be set to different bias voltages for maximum output power and efficiency. Even though the max DC voltage to the chip power supply is 12 V, in AC condition, do not provide over 6 V power supply to the chip.

9. TEST AND APPLICATION SCHEMATIC

The typical test and application circuit for 400MHz is shown in Fig.2 for SCT3604

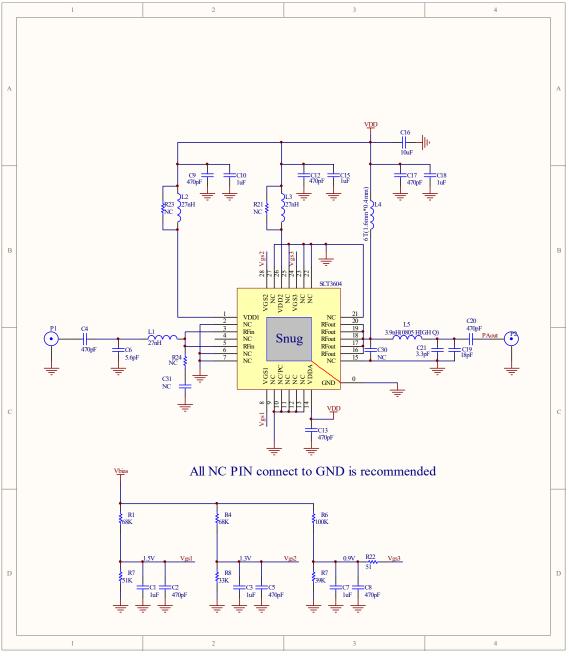
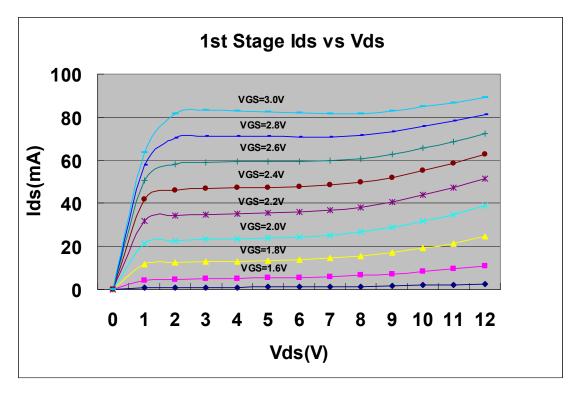
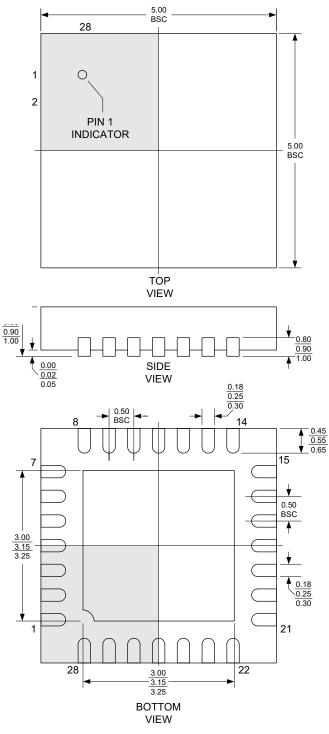


Fig.2. Test and application circuit





11. PACKAGING INFORMATION



Dimensions shown in millimeters Fig.4: 5x5mm QFN 28-pin package

12. DISCLAIMERS

- Life support applications These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Sicomm customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Sicomm for any damages resulting from such applications.
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