Tactical Grade, Ten Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16488A

FEATURES

- **Triaxial, digital gyroscope, ±450°/sec dynamic range**
  - **±0.05° orthogonal alignment error**
  - **5.1°/hr in-run bias stability**
  - **0.26°/√hr angular random walk**
  - **0.01% nonlinearity**
- **Triaxial, digital accelerometer, ±18 *g***
- **Triaxial, delta angle and delta velocity outputs**
- **Triaxial, digital magnetometer, ±2.5 gauss**
- **Digital pressure sensor, 300 mbar to 1100 mbar**
- **Fast start-up time, ~500 ms**
- **Factory-calibrated sensitivity, bias, and axial alignment**
  - **Calibration temperature range: −40°C to +85°C**
- **SPI-compatible serial interface**
- **Embedded temperature sensor**
- **Programmable operation and control**
  - **Automatic and manual bias correction controls**
  - **4 FIR filter banks, 120 configurable taps**
  - **Digital input/output: data-ready alarm indicator, external clock**
  - **Alarms for condition monitoring**
  - **Power-down/sleep mode for power management**
  - **Optional external sample clock input: up to 2.4 kHz**
  - **Single command self test**
- **Single-supply operation: 3.0 V to 3.6 V**
- **2000 *g* shock survivability**
- **Operating temperature range: −55°C to +105°C (CML)**

APPLICATIONS

- **Platform stabilization and control**
- **Navigation**
- **Personnel tracking**
- **Instrumentation**
- **Robotics**

GENERAL DESCRIPTION

The ADIS16488A *i*Sensor® device is a complete inertial system that includes a triaxis gyroscope, a triaxis accelerometer, triaxis magnetometer, and pressure sensor. Each inertial sensor in the ADIS16488A combines industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16488A provides a simple, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structure provide a simple interface for data collection and configuration control.

The ADIS16488A uses the same footprint and connector system as the ADIS16375, ADIS16480, and ADIS16485, which greatly simplifies the upgrade process. The ADIS16488A is packaged in a module that is approximately 47 mm × 44 mm × 14 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

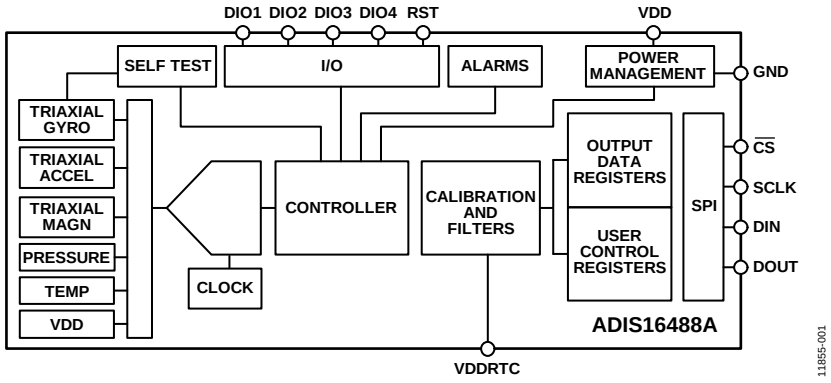

Figure 1.

Rev. F **Document Feedback**

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REVISION HISTORY

11/2018—Rev. E to Rev. F

Added Note 3 to Table 1; Renumbered Sequentially 5
Added X-Ray Sensitivity Section 35

9/2017—Rev. D to Rev. E

Changes to Logic Inputs Parameter, Table 1 5
Added Endnote 6, Table 1; Renumbered Sequentially 5
Changed PC-Based Evaluation, EVAL-ADIS Section Title to PC-Based Evaluation, EVAL-ADIS2 Section Title 35
Changes to PC-Based Evaluation, EVAL-ADIS2 Section 35

11/2016—Rev. C to Rev. D

Changes to Figure 29 and Figure 30 34
Change to Ordering Guide 35

8/2015—Rev. B to Rev. C

Changes to Table 72, Table 73, and Table 74 24
Changes to Table 82, Table 83, and Table 84 25

2/2015—Rev. A to Rev. B

Change to Features Section 1
Changes to t_2 Parameter, Table 2, and Figure 2 5
Added Table 3; Renumbered Sequentially 5
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Change to Dual Memory Structure Section 11
Change to Table 72, Table 73, and Table 74 24
Change to Table 82, Table 83, and Table 84 25

5/2014—Rev. 0 to Rev. A

Changes to Table 71, Table 72, and Table 73 23
Changes to Table 81, Table 82, and Table 83 24

1/2014—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±450°/sec ± 1 *g*, 300 mbar to 1100 mbar, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450		±480	°/sec
Sensitivity	x_GYRO_OUT and x_GYRO_LOW (32-bit)		3.052×10^{-7}		°/sec/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±1	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±35		ppm/°C
Misalignment	Axis to axis		±0.05		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, FS = 450°/sec		0.01		% of FS
Bias Repeatability[1, 2]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		°/sec
In-Run Bias Stability	1 σ		5.1		°/hr
Angular Random Walk	1 σ		0.26		°/√hr
Bias Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.0025		°/sec/°C
Linear Acceleration Effect on Bias	Any axis, 1 σ (CONFIG[7] = 1)		0.009		°/sec/*g*
Output Noise	No filtering		0.135		°/sec rms
Rate Noise Density	f = 10 Hz to 40 Hz, no filtering		0.0059		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			18		kHz
ACCELEROMETERS	Each axis				
Dynamic Range		±18			*g*
Sensitivity	x_ACCL_OUT and x_ACCL_LOW (32-bit)		1.221×10^{-8}		*g*/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±0.5	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±25		ppm/°C
Misalignment	Axis to axis		±0.035		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, ±10 *g*		0.1		% of FS
	Best fit straight line, ±18 *g*		0.5		% of FS
Bias Repeatability[1, 2, 3]	−40°C ≤ T_C ≤ +85°C, 1 σ		±16		m*g*
In-Run Bias Stability	1 σ		0.07		m*g*
Velocity Random Walk	1 σ		0.029		m/sec/√hr
Bias Temperature Coefficient	−40°C ≤ T_C ≤ +85°C		±0.1		m*g*/°C
Output Noise	No filtering		1.29		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		0.063		m*g*/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
MAGNETOMETER					
Dynamic Range		±2.5			gauss
Sensitivity			0.1		mgauss/LSB
Initial Sensitivity Tolerance				±2	%
Sensitivity Temperature Coefficient	ADIS16488BMLZ, −40°C ≤ T_C ≤ +85°C, 1 σ		275		ppm/°C
	ADIS16488CMLZ, −40°C ≤ T_C ≤ +85°C, 1 σ		60		ppm/°C
Misalignment	Axis to axis		0.35		Degrees
	Axis to frame (package)		1.0		Degrees
Nonlinearity	Best fit straight line		0.5		% of FS
Initial Bias Error	0 gauss stimulus		±15		mgauss
Bias Temperature Coefficient	ADIS16488BMLZ, −40°C ≤ T_C ≤ +85°C, 1 σ		0.3		mgauss/°C
	ADIS16488CMLZ, −40°C ≤ T_C ≤ +85°C, 1 σ		0.03		mgauss/°C
Output Noise	No filtering		0.22		mgauss rms
Noise Density	f = 2 Hz to 5 Hz, no filtering		0.042		mgauss/√Hz
3 dB Bandwidth			330		Hz
BAROMETER					
Pressure Range		300		1100	mbar
	Extended	10		1200	mbar
Sensitivity	BAROM_OUT and BAROM_LOW (32-bit)		6.1×10^{-7}		mbar/LSB
Error with Supply			0.04		%/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Total Error			4.5		mbar
Relative Error[4]	−40°C ≤ T_C ≤ +85°C		2.5		mbar
Nonlinearity[5]	Best fit straight line, FS = 1100 mbar		0.1		% of FS
	−40°C ≤ T_C ≤ +85°C		0.2		% of FS
Linear-*g* Sensitivity	±1 *g*, 1 σ		0.005		mbar/*g*
Noise			0.025		mbar rms
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.00565		°C/LSB
LOGIC INPUTS[6]					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
$\overline{CS}$ Wake-Up Pulse Width		20			µs
Logic 1 Input Current, I_{IH}	V_{IH} = 3.3 V			10	µA
Logic 0 Input Current, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$ and $\overline{CS}$				10	µA
$\overline{RST}$ and $\overline{CS}$ Pins[7]			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[8]	100,000			Cycles
Data Retention[9]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[10]	Time until data is available				
Power-On Start-Up Time			500		ms
Reset Recovery Time[11]			500		ms
Sleep Mode Recovery Time			500		µs
Flash Memory					
Update Time			375		ms
Test Time			50		ms
Automatic Self Test Time	Using internal clock, 100 SPS		12		ms
CONVERSION RATE			2.46		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock		0.7[12]		2.4	kHz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[13]	Normal mode, VDD = 3.3 V, µ ± σ		245		mA
	Sleep mode, VDD = 3.3 V		12.2		mA
	Power-down mode, VDD = 3.3 V		45		µA
POWER SUPPLY, VDDRTC	Operating voltage range	3.0		3.6	V
Real-Time Clock Supply Current	Normal mode, VDDRTC = 3.3 V		13		µA

[1] The repeatability specifications represent analytical projections based on the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: +110°C, 500 hours), drift from temperature cycling (JESD22, Method A104-C, Method N, 500 cycles, −55°C to +85°C), rate random walk (10-year projection), and broadband noise.
[2] Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability relates to the in-run bias stability and noise density specifications.
[3] X-ray exposure can degrade this performance metric.
[4] The relative error assumes that the initial error, at 25°C, is corrected in the end application.
[5] Specification assumes a full scale (FS) of 1000 mbar.
[6] The digital input/output signals use a 3.3 V system.
[7] $\overline{RST}$ and $\overline{CS}$ pins are connected to the VDD pin through 10 kΩ pull-up resistors.
[8] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[9] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[10] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.
[11] The $\overline{RST}$ line must be in a low state for at least 10 µs to assure a proper reset initiation and recovery.
[12] Device functions at clock rates below 0.7 kHz, but at reduced performance levels.
[13] Supply current transients can reach 600 mA during initial start up or reset recovery.

TIMING SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

		Normal Mode			
Parameter	**Description**	**Min[1]**	**Typ**	**Max[1]**	**Unit**
f_{SCLK}	Serial clock	0.01		15	MHz
t_{STALL}[2]	Stall period between data	2			µs
t_{CLS}	Serial clock low period	31			ns
t_{CHS}	Serial clock high period	31			ns
$t_{\overline{CS}}$	Chip select to clock edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise/fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to data out active	0		11	ns
t_{HD}	SCLK edge to data out invalid	0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to data out high impedance	0		9	ns
t_1	Input sync pulse width	5			µs
t_2	Input sync to data invalid		490		µs
t_3	Input sync period	417			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating.

Table 3. Register Specific Stall Times

Register	Function	Minimum Stall Time (µs)
FNCTIO_CTRL	Configure DIOx functions	15
FLTR_BNK0	Enable/select FIR filter banks	10
FLTR_BNK1	Enable/select FIR filter banks	10
NULL_CFG	Configure autonull bias function	10
GLOB_CMD[1]	Self-test	12,000
GLOB_CMD[2]	Flash memory test	50,000
GLOB_CMD[3]	Flash memory update	375,000
GLOB_CMD[6]	Factory calibration restore	75,000
GLOB_CMD[7]	Software reset	120,000

Timing Diagrams

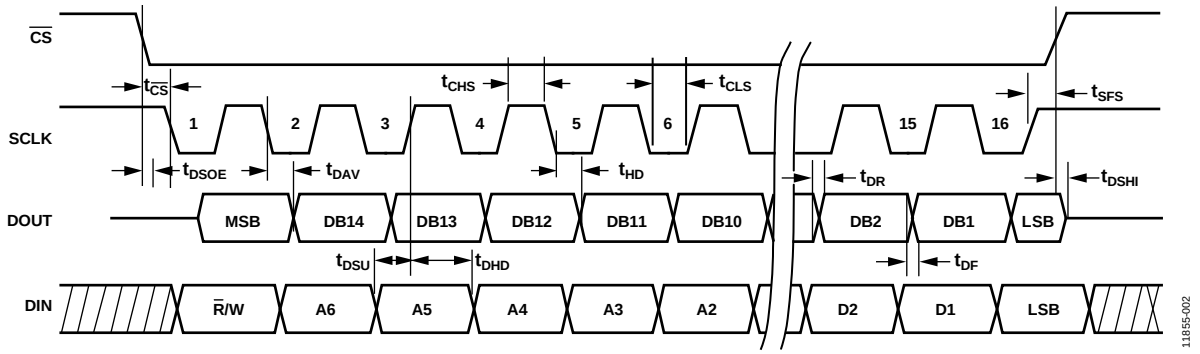

Figure 2. SPI Timing and Sequence

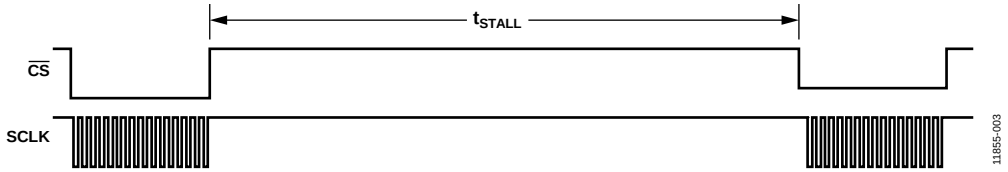

Figure 3. Stall Time and Data Rate

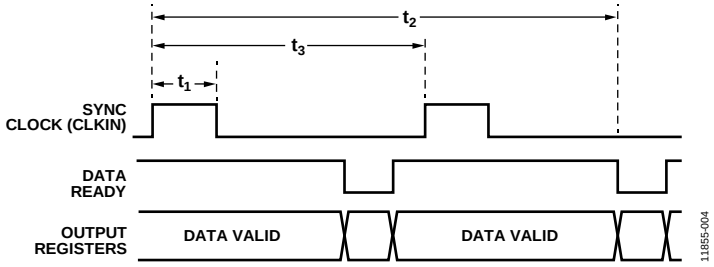

Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Operating Temperature Range	
ADIS16488BMLZ	−40°C to +105°C
ADIS16488CMLZ	−55°C to +105°C
Storage Temperature Range[1]	−65°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −55°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module (ML-24-6)	22.8°C/W	10.1°C/W	48 *g*

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

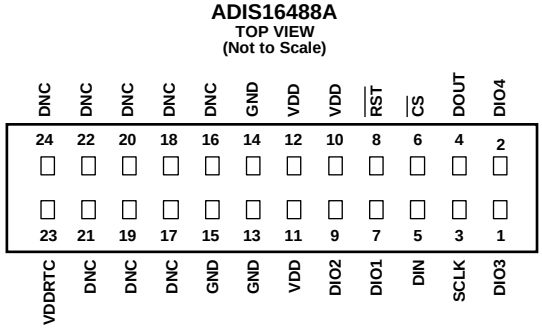

Figure 5. Mating Connector Pin Assignments

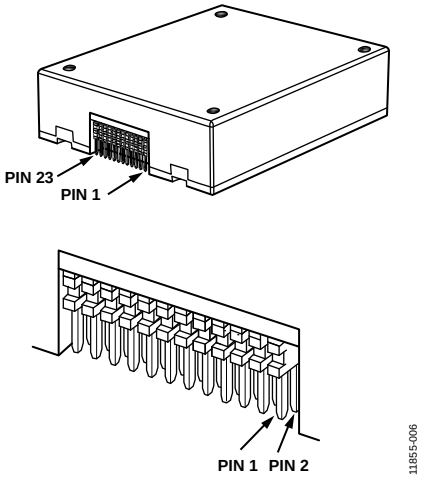

Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input/output	Configurable Digital Input/Output.
2	DIO4	Input/output	Configurable Digital Input/Output.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input/output	Configurable Digital Input/Output.
8	$\overline{RST}$	Input	Reset.
9	DIO2	Input/output	Configurable Digital Input/Output.
10, 11, 12	VDD	Supply	Power Supply.
13, 14, 15	GND	Supply	Power Ground.
16 to 22, 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
23	VDDRTC	Supply	Real-Time Clock Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

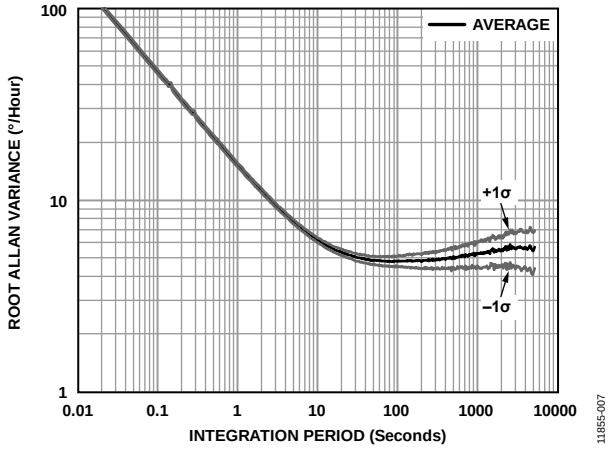

Figure 7. Gyroscope Allan Variance, 25°C

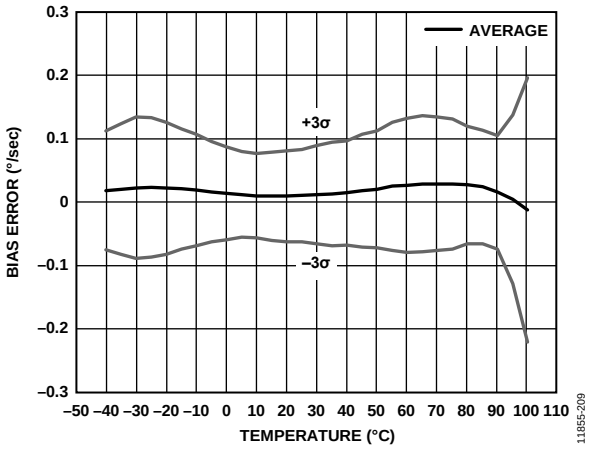

Figure 9. Gyroscope Bias Error vs. Temperature

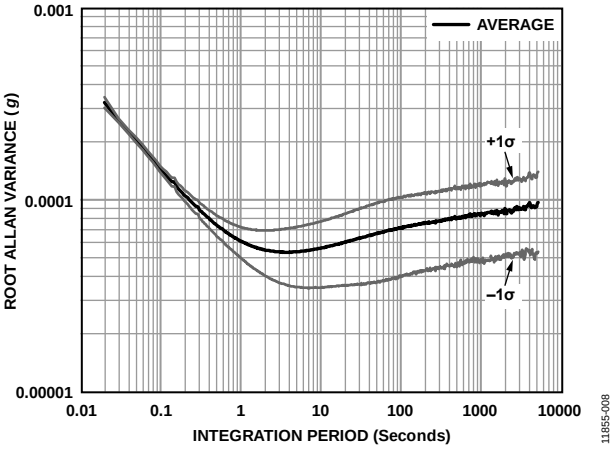

Figure 8. Accelerometer Allan Variance, 25°C

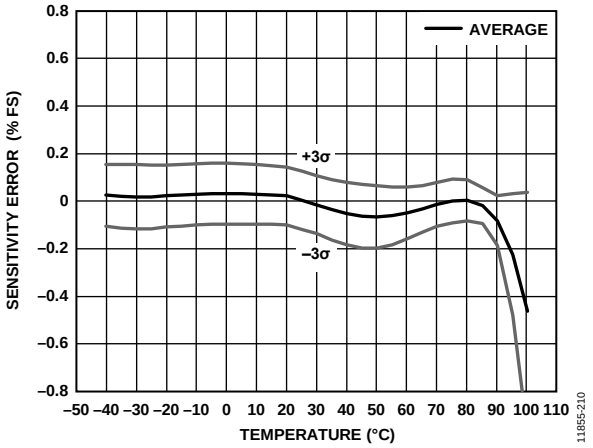

Figure 10. Gyroscope Scale (Sensitivity) Error vs. Temperature

THEORY OF OPERATION

The ADIS16488A is an autonomous sensor system that self starts when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor, using the connections as shown in Figure 11.

The four SPI signals facilitate synchronous, serial data communication. Connect the reset line ($\overline{RST}$) to VDD or do not connect it to anything for normal operation. The factory default configuration provides users with a data ready signal on the DIO2 pin, which pulses high when new data is available in the output data registers.

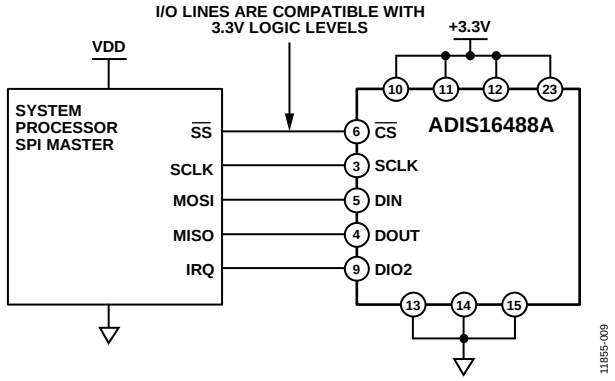

Figure 11. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices, such as the ADIS16488A. Table 8 provides a list of settings describing the SPI protocol of the ADIS16488A. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16488A operates as a slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), and CPHA = 1 (phase)
MSB-First Mode	Bit sequence
16-Bit Mode	Shift register/data length

REGISTER STRUCTURE

The register structure and SPI port provide a bridge between the sensor processing system and an external, master processor. It contains both output data and control registers. The output data registers include the latest sensor data, a real-time clock, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input/output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16488A and an external processor involves either reading or writing to one of the user registers.

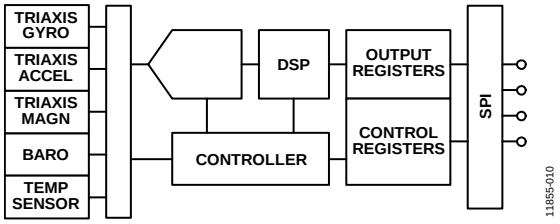

Figure 12. Basic Operation

The register structure uses a paged addressing scheme that is composed of 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence shown in Figure 13.

Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 9 displays the PAGE_ID contents for each page, together with their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 9. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, input/output, alarms
4	0x04	Serial number
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

SPI COMMUNICATION

If the previous command was a read request, the SPI port supports full duplex communication, which enables external processors to write to DIN while reading DOUT (see Figure 13). Figure 13 provides a guideline for the bit coding on both DIN and DOUT.

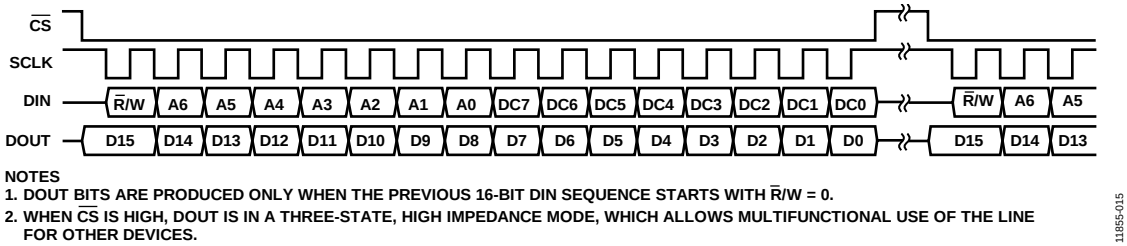

Figure 13. SPI Communication Bit Sequence

DEVICE CONFIGURATION

The SPI provides write access to the control registers, one byte at a time, using the bit assignments shown in Figure 13. Each register has 16 bits, where Bits[7:0] represent the lower address (listed in Table 10) and Bits[15:8] represent the upper address. Write to the lower byte of a register first, followed by a write to its upper byte (the only register that changes with a single write to its lower byte is the PAGE_ID register).

For a write command, the first bit in the DIN sequence is set to 1. Address Bits[A6:A0] represent the target address, and Data Command Bits[DC7:DC0] represent the data being written to the location. Figure 14 provides an example of writing 0x03 to Address 0x00 (PAGE_ID [7:0]) using DIN = 0x8003. This write command activates the control page for SPI access.

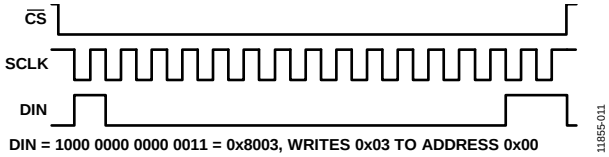

Figure 14. SPI Sequence for Activating the Control Page (DIN = 0x8003)

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, use the manual flash update command, which is located in GLOB_CMD[3] on Page 3 of the register map. Activate the manual flash update command by turning to Page 3 (DIN = 0x8003) and setting GLOB_CMD[3] = 1 (DIN = 0x8208, then DIN = 0x8300). For a flash memory update, ensure that the power supply is within specification for the entire processing time (see Table 1). Table 10 provides a memory map for all of the user registers, which includes a column of flash backup information. A yes in this column indicates that a register has a mirror location in flash and, when backed up properly, automatically restores itself during startup or after a reset. Figure 15 provides a diagram of the dual memory structure that supports all device operations and stores critical user settings.

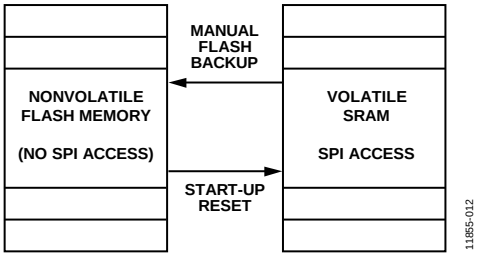

Figure 15. SRAM and Flash Memory Diagram

READING SENSOR DATA

The ADIS16488A automatically starts up and activates Page 0 for data register access. Write 0x00 to the PAGE_ID register (DIN = 0x8000) to activate Page 0 for data access after accessing any other page.

A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 13, and then the register contents follow DOUT during the second sequence.

The first bit in a DIN command is zero, followed by either the upper or lower address for the register. The last eight bits are don't care, but the SPI requires the full set of 16 SCLKs to receive the request.

Figure 16 includes two register reads in succession, which starts with DIN = 0x1A00, to request the contents of the Z_GYRO_OUT register, and follows with 0x1800, to request the contents of the Z_GYRO_LOW register.

Figure 16. SPI Read Example

Figure 17 provides an example of the four SPI signals when reading PROD_ID in a repeating pattern. This is an effective pattern to use for troubleshooting the SPI interface setup and communications because the contents of PROD_ID are predefined and stable.

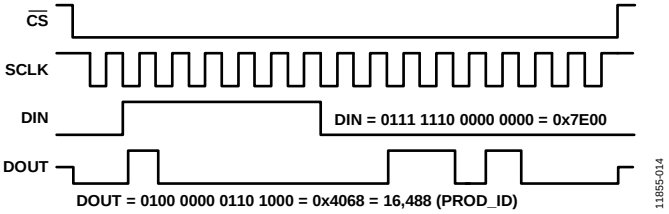

Figure 17. SPI Read Example, Second 16-Bit Sequence

USER REGISTERS

Table 10. User Register Memory Map (N/A = Not Applicable)

Name	R/W[1]	Flash	PAGE_ID	Address	Default	Register Description	Format
PAGE_ID	R/W	No	0x00	0x00	0x00	Page identifier	N/A
Reserved	N/A	N/A	0x00	0x02 to 0x04	N/A	Reserved	N/A
SEQ_CNT	R	No	0x00	0x06	N/A	Sequence counter	Table 57
SYS_E_FLAG	R	No	0x00	0x08	0x0000	Output, system error flags	Table 48
DIAG_STS	R	No	0x00	0x0A	0x0000	Output, self test error flags	Table 49
ALM_STS	R	No	0x00	0x0C	0x0000	Output, alarm error flags	Table 50
TEMP_OUT	R	No	0x00	0x0E	N/A	Output, temperature	Table 46
X_GYRO_LOW	R	No	0x00	0x10	N/A	Output, x-axis gyroscope, low word	Table 15
X_GYRO_OUT	R	No	0x00	0x12	N/A	Output, x-axis gyroscope, high word	Table 11
Y_GYRO_LOW	R	No	0x00	0x14	N/A	Output, y-axis gyroscope, low word	Table 16
Y_GYRO_OUT	R	No	0x00	0x16	N/A	Output, y-axis gyroscope, high word	Table 12
Z_GYRO_LOW	R	No	0x00	0x18	N/A	Output, z-axis gyroscope, low word	Table 17
Z_GYRO_OUT	R	No	0x00	0x1A	N/A	Output, z-axis gyroscope, high word	Table 13
X_ACCL_LOW	R	No	0x00	0x1C	N/A	Output, x-axis accelerometer, low word	Table 22
X_ACCL_OUT	R	No	0x00	0x1E	N/A	Output, x-axis accelerometer, high word	Table 18
Y_ACCL_LOW	R	No	0x00	0x20	N/A	Output, y-axis accelerometer, low word	Table 23
Y_ACCL_OUT	R	No	0x00	0x22	N/A	Output, y-axis accelerometer, high word	Table 19
Z_ACCL_LOW	R	No	0x00	0x24	N/A	Output, z-axis accelerometer, low word	Table 24
Z_ACCL_OUT	R	No	0x00	0x26	N/A	Output, z-axis accelerometer, high word	Table 20
X_MAGN_OUT	R	No	0x00	0x28	N/A	Output, x-axis magnetometer, high word	Table 39
Y_MAGN_OUT	R	No	0x00	0x2A	N/A	Output, y-axis magnetometer, high word	Table 40
Z_MAGN_OUT	R	No	0x00	0x2C	N/A	Output, z-axis magnetometer, high word	Table 41
BAROM_LOW	R	No	0x00	0x2E	N/A	Output, barometer, low word	Table 45
BAROM_OUT	R	No	0x00	0x30	N/A	Output, barometer, high word	Table 43
Reserved	N/A	N/A	0x00	0x32 to 0x3E	N/A	Reserved	N/A
X_DELTANG_LOW	R	No	0x00	0x40	N/A	Output, x-axis delta angle, low word	Table 29
X_DELTANG_OUT	R	No	0x00	0x42	N/A	Output, x-axis delta angle, high word	Table 25
Y_DELTANG_LOW	R	No	0x00	0x44	N/A	Output, y-axis delta angle, low word	Table 30
Y_DELTANG_OUT	R	No	0x00	0x46	N/A	Output, y-axis delta angle, high word	Table 26
Z_DELTANG_LOW	R	No	0x00	0x48	N/A	Output, z-axis delta angle, low word	Table 31
Z_DELTANG_OUT	R	No	0x00	0x4A	N/A	Output, z-axis delta angle, high word	Table 27
X_DELTVEL_LOW	R	No	0x00	0x4C	N/A	Output, x-axis delta velocity, low word	Table 36
X_DELTVEL_OUT	R	No	0x00	0x4E	N/A	Output, x-axis delta velocity, high word	Table 32
Y_DELTVEL_LOW	R	No	0x00	0x50	N/A	Output, y-axis delta velocity, low word	Table 37
Y_DELTVEL_OUT	R	No	0x00	0x52	N/A	Output, y-axis delta velocity, high word	Table 33
Z_DELTVEL_LOW	R	No	0x00	0x54	N/A	Output, z-axis delta velocity, low word	Table 38
Z_DELTVEL_OUT	R	No	0x00	0x56	N/A	Output, z-axis delta velocity, high word	Table 34
Reserved	N/A	N/A	0x00	0x58 to 0x76	N/A	Reserved	N/A
TIME_MS_OUT	R/W	Yes	0x00	0x78	N/A	Factory configuration time: minutes/seconds	Table 125
TIME_DH_OUT	R/W	Yes	0x00	0x7A	N/A	Factory configuration date/time: day/hour	Table 126
TIME_YM_OUT	R/W	Yes	0x00	0x7C	N/A	Factory configuration date: year/month	Table 127
PROD_ID	R	Yes	0x00	0x7E	0x4068	Output, product identification (16,488)	Table 54
Reserved	N/A	N/A	0x01	0x00 to 0x7E	N/A	Reserved	N/A
PAGE_ID	R/W	No	0x02	0x00	0x00	Page identifier	N/A
Reserved	N/A	N/A	0x02	0x02	N/A	Reserved	N/A
X_GYRO_SCALE	R/W	Yes	0x02	0x04	0x0000	Calibration, scale, x-axis gyroscope	Table 72
Y_GYRO_SCALE	R/W	Yes	0x02	0x06	0x0000	Calibration, scale, y-axis gyroscope	Table 73
Z_GYRO_SCALE	R/W	Yes	0x02	0x08	0x0000	Calibration, scale, z-axis gyroscope	Table 74
X_ACCL_SCALE	R/W	Yes	0x02	0x0A	0x0000	Calibration, scale, x-axis accelerometer	Table 82
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C	0x0000	Calibration, scale, y-axis accelerometer	Table 83

Name	R/W[1]	Flash	PAGE_ID	Address	Default	Register Description	Format
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E	0x0000	Calibration, scale, z-axis accelerometer	Table 84
XG_BIAS_LOW	R/W	Yes	0x02	0x10	0x0000	Calibration, offset, gyroscope, x-axis, low word	Table 68
XG_BIAS_HIGH	R/W	Yes	0x02	0x12	0x0000	Calibration, offset, gyroscope, x-axis, high word	Table 65
YG_BIAS_LOW	R/W	Yes	0x02	0x14	0x0000	Calibration, offset, gyroscope, y-axis, low word	Table 69
YG_BIAS_HIGH	R/W	Yes	0x02	0x16	0x0000	Calibration, offset, gyroscope, y-axis, high word	Table 66
ZG_BIAS_LOW	R/W	Yes	0x02	0x18	0x0000	Calibration, offset, gyroscope, z-axis, low word	Table 70
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A	0x0000	Calibration, offset, gyroscope, z-axis, high word	Table 67
XA_BIAS_LOW	R/W	Yes	0x02	0x1C	0x0000	Calibration, offset, accelerometer, x-axis, low word	Table 79
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E	0x0000	Calibration, offset, accelerometer, x-axis, high word	Table 76
YA_BIAS_LOW	R/W	Yes	0x02	0x20	0x0000	Calibration, offset, accelerometer, y-axis, low word	Table 80
YA_BIAS_HIGH	R/W	Yes	0x02	0x22	0x0000	Calibration, offset, accelerometer, y-axis, high word	Table 77
ZA_BIAS_LOW	R/W	Yes	0x02	0x24	0x0000	Calibration, offset, accelerometer, z-axis, low word	Table 81
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26	0x0000	Calibration, offset, accelerometer, z-axis, high word	Table 78
HARD_IRON_X	R/W	Yes	0x02	0x28	0x0000	Calibration, hard iron, magnetometer, x-axis	Table 85
HARD_IRON_Y	R/W	Yes	0x02	0x2A	0x0000	Calibration, hard iron, magnetometer, y-axis	Table 86
HARD_IRON_Z	R/W	Yes	0x02	0x2C	0x0000	Calibration, hard iron, magnetometer, z-axis	Table 87
SOFT_IRON_S11	R/W	Yes	0x02	0x2E	0x0000	Calibration, soft iron, magnetometer, S11	Table 89
SOFT_IRON_S12	R/W	Yes	0x02	0x30	0x0000	Calibration, soft iron, magnetometer, S12	Table 90
SOFT_IRON_S13	R/W	Yes	0x02	0x32	0x0000	Calibration, soft iron, magnetometer, S13	Table 91
SOFT_IRON_S21	R/W	Yes	0x02	0x34	0x0000	Calibration, soft iron, magnetometer, S21	Table 92
SOFT_IRON_S22	R/W	Yes	0x02	0x36	0x0000	Calibration, soft iron, magnetometer, S22	Table 93
SOFT_IRON_S23	R/W	Yes	0x02	0x38	0x0000	Calibration, soft iron, magnetometer, S23	Table 94
SOFT_IRON_S31	R/W	Yes	0x02	0x3A	0x0000	Calibration, soft iron, magnetometer, S31	Table 95
SOFT_IRON_S32	R/W	Yes	0x02	0x3C	0x0000	Calibration, soft iron, magnetometer, S32	Table 96
SOFT_IRON_S33	R/W	Yes	0x02	0x3E	0x0000	Calibration, soft iron, magnetometer, S33	Table 97
BR_BIAS_LOW	R/W	Yes	0x02	0x40	0x0000	Calibration, offset, barometer, low word	Table 100
BR_BIAS_HIGH	R/W	Yes	0x02	0x42	0x0000	Calibration, offset, barometer, high word	Table 99
Reserved	N/A	N/A	0x02	0x44 to 0x72	N/A	Reserved	N/A
USER_SCR_1	R/W	Yes	0x02	0x74	0x0000	User Scratch Register 1	Table 121
USER_SCR_2	R/W	Yes	0x02	0x76	0x0000	User Scratch Register 2	Table 122
USER_SCR_3	R/W	Yes	0x02	0x78	0x0000	User Scratch Register 3	Table 123
USER_SCR_4	R/W	Yes	0x02	0x7A	0x0000	User Scratch Register 4	Table 124
FLSHCNT_LOW	R	Yes	0x02	0x7C	N/A	Diagnostic, flash memory count, low word	Table 116
FLSHCNT_HIGH	R	Yes	0x02	0x7E	N/A	Diagnostic, flash memory count, high word	Table 117
PAGE_ID	R/W	No	0x03	0x00	0x0000	Page identifier	N/A
GLOB_CMD	W	No	0x03	0x02	N/A	Control, global commands	Table 115
Reserved	N/A	N/A	0x03	0x04	N/A	Reserved	N/A
FNCTIO_CTRL	R/W	Yes	0x03	0x06	0x000D	Control, input/output pins, functional definitions	Table 118
GPIO_CTRL	R/W	Yes	0x03	0x08	0x00X0[2]	Control, input/output pins, general purpose	Table 119
CONFIG	R/W	Yes	0x03	0x0A	0x00C0	Control, clock, and miscellaneous correction	Table 75
DEC_RATE	R/W	Yes	0x03	0x0C	0x0000	Control, output sample rate decimation	Table 56
NULL_CNFG	R/W	Yes	0x03	0x0E	0x070A	Control, automatic bias correction configuration	Table 71
SLP_CNT	R/W	No	0x03	0x10	N/A	Control, power-down/sleep mode	Table 120
Reserved	N/A	N/A	0x03	0x12 to 0x14	N/A	Reserved	N/A
FILTR_BNK_0	R/W	Yes	0x03	0x16	0x0000	Filter selection	Table 58
FILTR_BNK_1	R/W	Yes	0x03	0x18	0x0000	Filter selection	Table 59
Reserved	N/A	N/A	0x03	0x1A to 0x1E	N/A	Reserved	N/A
ALM_CNFG_0	R/W	Yes	0x03	0x20	0x0000	Alarm configuration	Table 111
ALM_CNFG_1	R/W	Yes	0x03	0x22	0x0000	Alarm configuration	Table 112
ALM_CNFG_2	R/W	Yes	0x03	0x24	0x0000	Alarm configuration	Table 113
Reserved	N/A	N/A	0x03	0x26	N/A	Reserved	N/A
XG_ALM_MAGN	R/W	Yes	0x03	0x28	0x0000	Alarm, x-axis gyroscope threshold setting	Table 101
YG_ALM_MAGN	R/W	Yes	0x03	0x2A	0x0000	Alarm, y-axis gyroscope threshold setting	Table 102

Name	R/W[1]	Flash	PAGE_ID	Address	Default	Register Description	Format
ZG_ALM_MAGN	R/W	Yes	0x03	0x2C	0x0000	Alarm, z-axis gyroscope threshold setting	Table 103
XA_ALM_MAGN	R/W	Yes	0x03	0x2E	0x0000	Alarm, x-axis accelerometer threshold	Table 104
YA_ALM_MAGN	R/W	Yes	0x03	0x30	0x0000	Alarm, y-axis accelerometer threshold	Table 105
ZA_ALM_MAGN	R/W	Yes	0x03	0x32	0x0000	Alarm, z-axis accelerometer threshold	Table 106
XM_ALM_MAGN	R/W	Yes	0x03	0x34	0x0000	Alarm, x-axis magnetometer threshold	Table 107
YM_ALM_MAGN	R/W	Yes	0x03	0x36	0x0000	Alarm, y-axis magnetometer threshold	Table 108
ZM_ALM_MAGN	R/W	Yes	0x03	0x38	0x0000	Alarm, z-axis magnetometer threshold	Table 109
BR_ALM_MAGN	R/W	Yes	0x03	0x3A	0x0000	Alarm, barometer threshold setting	Table 110
Reserved	N/A	N/A	0x03	0x3C to 0x76	N/A	Reserved	N/A
FIRM_REV	R	Yes	0x03	0x78	N/A	Firmware revision	Table 51
FIRM_DM	R	Yes	0x03	0x7A	N/A	Firmware programming date: day/month	Table 52
FIRM_Y	R	Yes	0x03	0x7C	N/A	Firmware programming date: year	Table 53
Reserved	N/A	N/A	0x03	0x7E	N/A	Reserved	N/A
Reserved	N/A	N/A	0x04	0x00 to 0x18	N/A	Reserved	N/A
SERIAL_NUM	R	Yes	0x04	0x20	N/A	Serial number	Table 55
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved	N/A
PAGE_ID	R/W	No	0x05	0x00	0x0000	Page identifier	N/A
FIR_COEF_Axxx	R/W	Yes	0x05	0x02 to 0x7E	N/A	FIR Filter Bank A, Coefficient 0 through Coefficient 59	Table 60
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier	N/A
FIR_COEF_Axxx	R/W	Yes	0x06	0x02 to 0x7E	N/A	FIR Filter Bank A, Coefficient 60 through Coefficient 119	Table 60
PAGE_ID	R/W	No	0x07	0x00	0x0000	Page identifier	N/A
FIR_COEF_Bxxx	R/W	Yes	0x07	0x02 to 0x7E	N/A	FIR Filter Bank B, Coefficient 0 through Coefficient 59	Table 61
PAGE_ID	R/W	No	0x08	0x00	0x0000	Page identifier	N/A
FIR_COEF_Bxxx	R/W	Yes	0x08	0x02 to 0x7E	N/A	FIR Filter Bank B, Coefficient 60 through Coefficient 119	Table 61
PAGE_ID	R/W	No	0x09	0x00	0x0000	Page identifier	N/A
FIR_COEF_Cxxx	R/W	Yes	0x09	0x02 to 0x7E	N/A	FIR Filter Bank C, Coefficient 0 through Coefficient 59	Table 62
PAGE_ID	R/W	No	0x0A	0x00	0x0000	Page identifier	N/A
FIR_COEF_Cxxx	R/W	Yes	0x0A	0x02 to 0x7E	N/A	FIR Filter Bank C, Coefficient 60 through Coefficient 119	Table 62
PAGE_ID	R/W	No	0x0B	0x00	0x0000	Page identifier	N/A
FIR_COEF_Dxxx	R/W	Yes	0x0B	0x02 to 0x7E	N/A	FIR Filter Bank D, Coefficient 0 through Coefficient 59	Table 63
PAGE_ID	R/W	No	0x0C	0x00	0x0000	Page identifier	N/A
FIR_COEF_Dxxx	R/W	Yes	0x0C	0x02 to 0x7E	N/A	FIR Filter Bank D, Coefficient 60 through Coefficient 119	Table 63

[1] R is read only, W is write only, R/W is read and write, and N/A means not applicable.
[2] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

OUTPUT DATA REGISTERS

After the ADIS16488A completes its start-up process, the PAGE_ID register contains 0x0000, which sets Page 0 as the active page for SPI access. Page 0 contains the output data, real-time clock, status, and product identification registers.

INERTIAL SENSOR DATA FORMAT

The gyroscope, accelerometer, delta angle, delta velocity, and barometer output data registers use a 32-bit, twos complement format. Each output uses two registers to support this resolution. Figure 18 provides an example of how each register contributes to each inertial measurement. In this case, X_GYRO_OUT is the most significant word (upper 16 bits), and X_GYRO_LOW is the least significant word (lower 16 bits). In many cases, using the most significant word registers alone provides sufficient resolution for preserving key performance metrics.

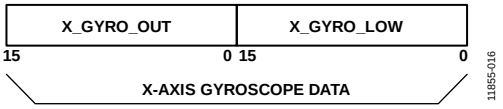

Figure 18. Gyroscope Output Format Example, DEC_RATE > 0

The arrows in Figure 19 represent the direction of the motion, which produces a positive output response in the output register of each sensor. The accelerometers respond to both dynamic and static forces associated with acceleration, including gravity. When lying perfectly flat, as shown in Figure 19, the z-axis accelerometer output is 1 *g*, and the x and y accelerometers are 0 *g*.

ROTATION RATE (GYROSCOPE)

The registers that use the x_GYRO_OUT format are the primary registers for the gyroscope measurements (see Table 11, Table 12, and Table 13). When processing data from these registers, use a 16-bit, twos complement data format. Table 14 provides x_GYRO_OUT digital coding examples.

Table 11. X_GYRO_OUT (Page 0, Base Address = 0x12)

Bits	Description
[15:0]	X-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 12. Y_GYRO_OUT (Page 0, Base Address = 0x16)

Bits	Description
[15:0]	Y-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 13. Z_GYRO_OUT (Page 0, Base Address = 0x1A)

Bits	Description
[15:0]	Z-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 14. x_GYRO_OUT Data Format Examples

Rotation Rate	Decimal	Hex	Binary
+450°/sec	+22,500	0x57E4	0101 0111 1110 0100
+0.04/sec	+2	0x0002	0000 0000 0000 0010
+0.02°/sec	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
−0.02°/sec	−1	0xFFFF	1111 1111 1111 1111
−0.04°/sec	−2	0xFFFE	1111 1111 1111 1110
−450°/sec	−22,500	0xA81C	1010 1000 0001 1100

The registers that use the x_GYRO_LOW naming format provide additional resolution for the gyroscope measurements (see Table 15, Table 16, and Table 17). The MSB has a weight of 0.01°/sec, and each subsequent bit has ½ the weight of the previous one.

Table 15. X_GYRO_LOW (Page 0, Base Address = 0x10)

Bits	Description
[15:0]	X-axis gyroscope data; additional resolution bits

Table 16. Y_GYRO_LOW (Page 0, Base Address = 0x14)

Bits	Description
[15:0]	Y-axis gyroscope data; additional resolution bits

Table 17. Z_GYRO_LOW (Page 0, Base Address = 0x18)

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

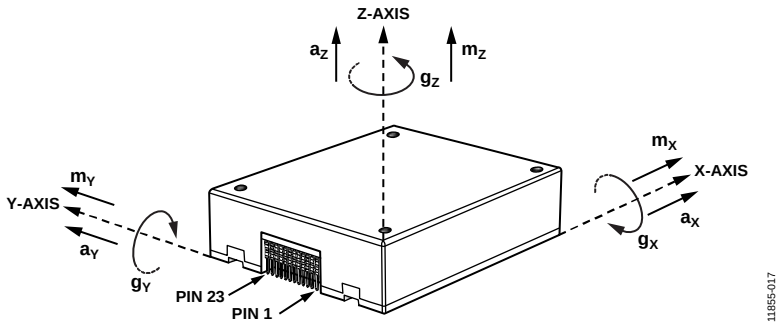

Figure 19. Inertial Sensor Direction Reference Diagram

ACCELERATION

The registers that use the x_ACCL_OUT format are the primary registers for the accelerometer measurements (see Table 18, Table 19, and Table 20). When processing data from these registers, use a 16-bit, twos complement data format. Table 21 provides x_ACCL_OUT digital coding examples.

Table 18. X_ACCL_OUT (Page 0, Base Address = 0x1E)

Bits	Description
[15:0]	X-axis accelerometer data; twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 19. Y_ACCL_OUT (Page 0, Base Address = 0x22)

Bits	Description
[15:0]	Y-axis accelerometer data; twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 20. Z_ACCL_OUT (Page 0, Base Address = 0x26)

Bits	Description
[15:0]	Z-axis accelerometer data; twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 21. x_ACCL_OUT Data Format Examples

Acceleration	Decimal	Hex	Binary
+18 *g*	+22,500	0x57E4	0101 0111 1110 0100
+1.6 m*g*	+2	0x0002	0000 0000 0000 0010
+0.8 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.8 m*g*	−1	0xFFFF	1111 1111 1111 1111
−1.6 m*g*	−2	0xFFFE	1111 1111 1111 1110
−18 *g*	−22,500	0xA81C	1010 1000 0001 1100

The registers that use the x_ACCL_LOW naming format provide additional resolution for the accelerometer measurements (see Table 22, Table 23, and Table 24). The MSB has a weight of 0.4 mg, and each subsequent bit has ½ the weight of the previous one.

Table 22. X_ACCL_LOW (Page 0, Base Address = 0x1C)

Bits	Description
[15:0]	X-axis accelerometer data; additional resolution bits

Table 23. Y_ACCL_LOW (Page 0, Base Address = 0x20)

Bits	Description
[15:0]	Y-axis accelerometer data; additional resolution bits

Table 24. Z_ACCL_LOW (Page 0, Base Address = 0x24)

Bits	Description
[15:0]	Z-axis accelerometer data; additional resolution bits

DELTA ANGLES

The x_DELTANG_OUT registers are the primary output registers for the delta angle calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 25, Table 26, and Table 27). Table 28 provides x_DELTANG_OUT digital coding examples.

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1}\left(\omega_{x,nD+d} + \omega_{x,nD+d-1}\right)$$

where:

D is the decimation rate = DEC_RATE + 1.

fs is the sample rate.

d is the incremental variable in the summation formula.

ω_x is the x-axis rate of rotation (gyroscope).

n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x_DELTANG_xxx registers at high rotation rates. See Table 56 and Figure 20 for more information on the DEC_RATE register (decimation filter).

The x_DELTANG_LOW registers (see Table 29, Table 30, and Table 31) provide additional resolution bits for the delta angle and combine with the x_DELTANG_OUT registers to provide a 32-bit, twos complement number. The MSB in the x_DELTANG_LOW registers have a weight of ~0.011° (720°/2^{16}), and each subsequent bit carries a weight of ½ of the previous one.

Table 25. X_DELTANG_OUT (Page 0, Base Address = 0x42)

Bits	Description
[15:0]	X-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Table 26. Y_DELTANG_OUT (Page 0, Base Address = 0x46)

Bits	Description
[15:0]	Y-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Table 27. Z_DELTANG_OUT (Page 0, Base Address = 0x4A)

Bits	Description
[15:0]	Z-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

Table 28. x_DELTANG_OUT Data Format Examples

Angle (°)	Decimal	Hex	Binary
+720 × (2^{15} − 1)/2^{15}	+32,767	0x7FFF	0111 1111 1110 1111
+1440/2^{15}	+2	0x0002	0000 0000 0000 0010
+720/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−720/2^{15}	−1	0xFFFF	1111 1111 1111 1111
−1440/2^{15}	−2	0xFFFE	1111 1111 1111 1110
−720	−32,768	0x8000	1000 0000 0000 0000

Table 29. X_DELTANG_LOW (Page 0, Base Address = 0x40)

Bits	Description
[15:0]	X-axis delta angle data; additional resolution bits

Table 30. Y_DELTANG_LOW (Page 0, Base Address = 0x44)

Bits	Description
[15:0]	Y-axis delta angle data; additional resolution bits

Table 31. Z_DELTANG_LOW (Page 0, Base Address = 0x48)

Bits	Description
[15:0]	Z-axis delta angle data; additional resolution bits

DELTA VELOCITY

The registers that use the x_DELTVEL_OUT format are the primary registers for the delta velocity calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 32, Table 33, and Table 34). Table 35 provides x_DELTVEL_OUT digital coding examples.

The delta velocity outputs represent an integration of the accelerometer measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:

D is the decimation rate = DEC_RATE + 1.

f_S is the sample rate.

d is the incremental variable in the summation formula.

a_x is the x-axis linear acceleration.

n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x_DELTVEL_xxx registers at high rotation rates. See Table 56 and Figure 20 for more information on the DEC_RATE register (decimation filter).

Table 32. X_DELTVEL_OUT (Page 0, Base Address = 0x4E)

Bits	Description
[15:0]	X-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Table 33. Y_DELTVEL_OUT (Page 0, Base Address = 0x52)

Bits	Description
[15:0]	Y-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Table 34. Z_DELTVEL_OUT (Page 0, Base Address = 0x56)

Bits	Description
[15:0]	Z-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

Table 35. x_DELTVEL_OUT, Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
+200 × (2^{15} − 1)/2^{15}	+32,767	0x7FFF	0111 1111 1111 1111
+400/2^{15}	+2	0x0002	0000 0000 0000 0010
+200/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−200/2^{15}	−1	0xFFFF	1111 1111 1111 1111
−400/2^{15}	−2	0xFFFE	1111 1111 1111 1110
−200	−32,768	0x8000	1000 0000 0000 0000

The x_DELTVEL_LOW registers (see Table 36, Table 37, and Table 38) provide additional resolution bits for the delta velocity and combine with the x_DELTVEL_OUT registers to provide a 32-bit, twos complement number. The MSB in the x_DELTVEL_LOW registers have a weight of ~3.052 mm/sec (200 m/sec ÷ 2^{16}), and each subsequent bit carries a weight of ½ of the previous one.

Table 36. X_DELTVEL_LOW (Page 0, Base Address = 0x4C)

Bits	Description
[15:0]	X-axis delta velocity data; additional resolution bits

Table 37. Y_DELTVEL_LOW (Page 0, Base Address = 0x50)

Bits	Description
[15:0]	Y-axis delta velocity data; additional resolution bits

Table 38. Z_DELTVEL_LOW (Page 0, Base Address = 0x54)

Bits	Description
[15:0]	Z-axis delta velocity data; additional resolution bits

MAGNETOMETERS

The registers that use the x_MAGN_OUT format are the primary registers for the magnetometer measurements. When processing data from these registers, use a 16-bit, twos complement data format. Table 39, Table 40, and Table 41 provide the numerical format for each register, and Table 42 provides x_MAGN_OUT digital coding examples.

Table 39. X_MAGN_OUT (Page 0, Base Address = 0x28)

Bits	Description
[15:0]	X-axis magnetometer data; twos complement, ±3.2767 gauss range, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 40. Y_MAGN_OUT (Page 0, Base Address = 0x2A)

Bits	Description
[15:0]	Y-axis magnetometer data; twos complement, ±3.2767 gauss range, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 41. Z_MAGN_OUT (Page 0, Base Address = 0x2C)

Bits	Description
[15:0]	Z-axis magnetometer data; twos complement, ±3.2767 gauss range, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 42. x_MAGN_OUT Data Format Examples

Magnetic Field	Decimal	Hex	Binary
+3.2767 gauss	+32,767	0x7FFF	0111 1111 1111 1111
+0.2 mgauss	+2	0x0002	0000 0000 0000 0010
+0.1 mgauss	+1	0x0001	0000 0000 0000 0001
0 gauss	0	0x0000	0000 0000 0000 0000
−0.1 mgauss	−1	0xFFFF	1111 1111 1111 1111
−0.2 mgauss	−2	0xFFFE	1111 1111 1111 1110
−3.2768 gauss	−32,768	0x8000	1000 0000 0000 0000

BAROMETER

The BAROM_OUT register (see Table 43) and BAROM_LOW register (see Table 45) provide access to the barometric pressure data. These two registers combine to provide a 32-bit, twos complement format. Some applications can use BAROM_OUT by itself. For cases where the finer resolution available from BAROM_LOW is valuable, combine them in the same manner as the gyroscopes (see Figure 18). When processing data from the BAROM_OUT register alone, use a 16-bit, twos complement data format. Table 43 provides the numerical format for BAROM_OUT, and Table 44 provides digital coding examples.

Table 43. BAROM_OUT (Page 0, Base Address = 0x30)

Bits	Description
[15:0]	Barometric pressure; twos complement, ±1.31 bar range, 0 bar = 0x0000, 40 µbar/LSB

Table 44. BAROM_OUT Data Format Examples

Pressure (Bar)	Decimal	Hex	Binary
$+0.00004 \times (2^{15} - 1)$	+32,767	0x7FFF	0111 1111 1110 1111
+0.00008	+2	0x0002	0000 0000 0000 0010
+0.00004	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.00004	−1	0xFFFF	1111 1111 1111 1111
−0.00008	−2	0xFFFE	1111 1111 1111 1110
-0.00004×2^{15}	−32,768	0x8000	1000 0000 0000 0000

The BAROM_LOW register provides additional resolution for the barometric pressure measurement. The MSB has a weight of 20 µbar, and each subsequent bit carries a weight of ½ of the previous one.

Table 45. BAROM_LOW (Page 0, Base Address = 0x2E)

Bits	Description
[15:0]	Barometric pressure; additional resolution bits

INTERNAL TEMPERATURE

The TEMP_OUT register provides an internal temperature measurement for observing relative temperature changes inside the ADIS16488A (see Table 46). Table 47 provides TEMP_OUT digital coding examples. Note that this temperature reflects a higher temperature than that of ambient temperature, due to self heating.

Table 46. TEMP_OUT (Page 0, Base Address = 0x0E)

Bits	Description
[15:0]	Temperature data; twos complement, 0.00565°C per LSB, 25°C = 0x0000

Table 47. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+10,619	0x297B	0010 1001 0111 1011
+25 + 0.0113	+2	0x0002	0000 0000 0000 0010
+25 + 0.00565	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 − 0.00565	−1	0xFFFF	1111 1111 1111 1111
+25 − 0.0113	−2	0xFFFE	1111 1111 1111 1110
−40	−11,504	0xD310	1101 0011 0001 0000

STATUS/ALARM INDICATORS

The SYS_E_FLAG register in Table 48 provides the system error flags and new data bits for the magnetometer and barometer outputs. The new data flags trigger data collection of the magnetometer and barometer (x_MAGN_OUT and BAROM_xxx registers) because they update at a fixed rate that is not dependent on the DEC_RATE setting.

Reading the SYS_E_FLAG register clears all of its error flags and returns each bit to a zero value, with the exception of Bit 7. If SYS_E_FLAG[7] is high, use the software reset (GLOB_CMD[7] (see Table 115) to clear this condition and restore normal operation. If any bit in the SYS_E_FLAG register is associated with an error condition that remains after reading this register, this bit automatically returns to an alarm value of 1.

Table 48. SYS_E_FLAG (Page 0, Base Address = 0x08)

Bits	Description (Default = 0x0000)
[15]	Watch dog timer flag (1 = timed out)
[14:10]	Not used
9	New data flag, barometer (1 = new, unread data)[1]
8	New data flag, magnetometer (1 = new, unread data)[2]
7	Processing overrun (1 = error)
6	Flash memory update, result of GLOB_CMD[3] = 1 (1 = failed update, 0 = update successful)
5	Inertial self-test failure (1 = DIAG_STS ≠ 0x0000)
4	Sensor overrange (1 = at least one sensor overranged)
3	SPI communication error (1 = error condition, when the number of SCLK pulses is not equal to a multiple of 16)
[2:1]	Not used
0	Alarm status flag (1 = ALM_STS ≠ 0x0000)

[1] This flag restores to zero after reading the contents on BAROM_OUT.
[2] This flag restores to zero after reading one x_MAGN_OUT register.

The DIAG_STS register in Table 49 provides the flags for the internal self test function, which is from GLOB_CMD[1] (see Table 115). Note that the flag of the barometer, DIAG_STS[11], updates only after start-up and reset operations and that reading the DIAG_STS register causes all of its bits to restore to 0. The bits only return to 1 if the error condition persists.

Table 49. DIAG_STS (Page 0, Base Address = 0x0A)

Bits	Description (Default = 0x0000)
[15:12]	Not used
11	Self test failure, barometer (1 = failed at start-up)
10	Self test failure, z-axis magnetometer (1 = failure)
9	Self test failure, y-axis magnetometer (1 = failure)
8	Self test failure, x-axis magnetometer (1 = failure)
[7:6]	Not used
5	Self test failure, z-axis accelerometer (1 = failure)
4	Self test failure, y-axis accelerometer (1 = failure)
3	Self test failure, x-axis accelerometer (1 = failure)
2	Self test failure, z-axis gyroscope (1 = failure)
1	Self test failure, y-axis gyroscope (1 = failure)
0	Self test failure, x-axis gyroscope (1 = failure)

The ALM_STS register in Table 50 provides the alarm bits for the programmable alarm levels of each sensor. Note that reading the ALM_STS register causes all of its bits to restore to 0. The bits only return to 1 if the error condition persists.

Table 50. ALM_STS (Page 0, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:12]	Not used
11	Barometer alarm flag (1 = alarm is active)
10	Z-axis magnetometer alarm flag (1 = alarm is active)
9	Y-axis magnetometer alarm flag (1 = alarm is active)
8	X-axis magnetometer alarm flag (1 = alarm is active)
[7:6]	Not used
5	Z-axis accelerometer alarm flag (1 = alarm is active)
4	Y-axis accelerometer alarm flag (1 = alarm is active)
3	X-axis accelerometer alarm flag (1 = alarm is active)
2	Z-axis gyroscope alarm flag (1 = alarm is active)
1	Y-axis gyroscope alarm flag (1 = alarm is active)
0	X-axis gyroscope alarm flag (1 = alarm is active)

FIRMWARE REVISION

The FIRM_REV register (see Table 51) provides the firmware revision for the internal firmware. This register uses a binary coded decimal (BCD) format, where each nibble represents a digit. For example, if FIRM_REV = 0x1234, the firmware revision is 12.34. The tens digit is equal to 1, the ones digit is equal to 2, the tenths digit is equal to 3, and the hundredths digit is equal to 4.

Table 51. FIRM_REV (Page 3, Base Address = 0x78)

Bits	Description
[15:12]	Firmware revision BCD code, tens digit Numerical format = 4-bit binary, range = 0 to 9
[11:8]	Firmware revision BCD code, ones digit Numerical format = 4-bit binary, range = 0 to 9
[7:4]	Firmware revision BCD code, tenths digit Numerical format = 4-bit binary, range = 0 to 9
[3:0]	Firmware revision BCD code, hundredths digit Numerical format = 4-bit binary, range = 0 to 9

The FIRM_DM register (see Table 52) contains the month and day of the factory configuration date. FIRM_DM[15:12] and FIRM_DM[11:8] contain digits that represent the month of the factory configuration in a BCD format. For example, November is the 11th month in a year and is represented by FIRM_DM[15:8] = 0x11.

FIRM_DM[7:4] and FIRM_DM[3:0] contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by FIRM_DM[7:0] = 0x27.

Table 52. FIRM_DM (Page 3, Base Address = 0x7A)

Bits	Description
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration day BCD code, tens digit Numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit Numerical format = 4-bit binary, range = 0 to 9

The FIRM_Y register (see Table 53) contains the year of the factory configuration date. For example, the year, 2013, is represented by FIRM_Y = 0x2013.

Table 53. FIRM_Y (Page 3, Base Address = 0x7C)

Bits	Description
[15:12]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

PRODUCT IDENTIFICATION

The PROD_ID register (see Table 54) contains the binary equivalent of the device number (16,488 = 0x4068), and the SERIAL_NUM register (see Table 55) contains a lot-specific serial number.

Table 54. PROD_ID (Page 0, Base Address = 0x7E)

Bits	Description (Default = 0x4068)
[15:0]	Product identification = 0x4068

Table 55. SERIAL_NUM (Page 4, Base Address = 0x20)

Bits	Description
[15:0]	Lot-specific serial number

DIGITAL SIGNAL PROCESSING

GYROSCOPES/ACCELEROMETERS

Figure 20 provides a signal flow diagram for all of the components and settings that influence the frequency response for the accelerometers and gyroscopes. The sample rate for each accelerometer and gyroscope is 9.84 kHz. Each sensor has its own averaging/decimation filter stage, which reduces the update rate to 2.46 kSPS. When using the external clock option (FNCTIO_CTRL[7:4], see Table 118), the input clock drives a four-sample burst at a sample rate of 9.84 kSPS, which feeds into the 4× averaging/decimation filter. This results in a data rate that is equal to the input clock frequency.

AVERAGING/DECIMATION FILTER

The DEC_RATE register (see Table 56) provides user control for the final filter stage (see Figure 20), which averages and decimates the accelerometers, gyroscopes, delta angle, and delta velocity data. The output sample rate is equal to 2460/(DEC_RATE + 1).

When using the external clock option (FNCTIO_CTRL[7:4], see Table 118), replace the 2460 number in this relationship with the input clock frequency. For example, turn to Page 3 (DIN = 0x8003), and set DEC_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS (2460 ÷ 25).

Table 56. DEC_RATE (Page 3, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 2047, see Figure 20 for impact on sample rate

MAGNETOMETER/BAROMETER

When using the internal sampling clock, the magnetometer output registers (x_MAGN_OUT) update at a rate of 102.5 SPS and the barometer output registers (BAROM_xxx) update at a rate of 51.25 SPS. When using the external clock, the magnetometers update at a rate of 1/24th of the input clock frequency and the barometers update at a rate that is 1/48th of the input clock frequency.

The update rates for the magnetometer and barometers do not change with the DEC_RATE register settings. SYS_E_FLAG[9:8] (see Table 48) offers new data indicator bits that indicate fresh, unread data is in the x_MAGN_OUT and BAROM_xxx registers. The SEQ_CNT register provides a counter function to help determine when there is new data in the magnetometer and barometer registers.

When SEQ_CNT = 0x0001, there is new data in the magnetometer and barometer output registers. During initialization, the SEQ_CNT register helps to synchronize read loops for new data in both magnetometer and barometer outputs. When beginning a continuous read loop, read SEQ_CNT, then subtract this value from the maximum value shown (range) in Table 57 to predict the number of internal sample cycles until both magnetometer and barometer registers contain new data samples.

Table 57. SEQ_CNT (Page 0, Base Address = 0x06)

Bits	Description
[15:11]	Don't care
[6:0]	Binary counter: range = 1 to 48/(DEC_RATE + 1)

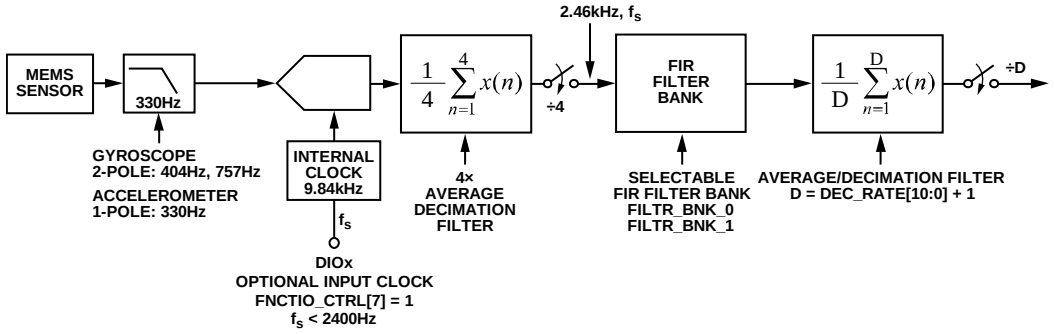

Figure 20. Sampling and Frequency Response Signal Flow

FIR FILTER BANKS

The ADIS16488A provides four configurable, 120-tap FIR filter banks. Each coefficient is 16 bits wide and occupies its own register location for each page. When designing a FIR filter for these banks, use a sample rate of 2.46 kHz and scale the coefficients so that their sum equals 32,768. For filter designs that have less than 120 taps, load the coefficients into the lower portion of the filter and start with Coefficient 1. To prevent adding phase delay to the response, ensure that all unused taps are equal to zero.

The FILTR_BNK_x registers provide three bits per sensor, which configure the filter bank (A, B, C, D) and turn filtering on and off. For example, turn to Page 3 (DIN = 0x8003), then write 0x0057 to FILTR_BNK_0 (DIN = 0x9657, DIN = 0x9700) to set the x-axis gyroscope to use the FIR filter in Bank D, to set the y-axis gyroscope to use the FIR filter in Bank B, and to enable these FIR filters in both x- and y-axis gyroscopes. Note that the filter settings update after writing to the upper byte; therefore, always configure the lower byte first. In cases that require configuration to only the lower byte of either FILTR_BNK_0 or FILTR_BNK_1, complete the process by writing 0x00 to the upper byte.

Table 58. FILTR_BNK_0 (Page 3, Base Address = 0x16)

Bits	Description (Default = 0x0000)
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Table 59. FILTR_BNK_1 (Page 3, Base Address = 0x18)

Bits	Description (Default = 0x0000)
[15:12]	Don't care
11	Z-axis magnetometer filter enable (1 = enabled)
[10:9]	Z-axis magnetometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Y-axis magnetometer filter enable (1 = enabled)
[7:6]	Y-axis magnetometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	X-axis magnetometer filter enable (1 = enabled)
[4:3]	X-axis magnetometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Filter Memory Organization

Each filter bank uses two pages of the user register structure. See Table 60, Table 61, Table 62, and Table 63 for the register addresses in each filter bank.

Table 60. Filter Bank A Memory Map

Page	PAGE_ID	Address	Register
5	0x05	0x00	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08	FIR_COEF_A000
5	0x05	0x0A	FIR_COEF_A001
5	0x05	0x0C to 0x7C	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E	FIR_COEF_A059
6	0x06	0x00	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08	FIR_COEF_A060
6	0x06	0x0A	FIR_COEF_A061
6	0x06	0x0C to 0x7C	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E	FIR_COEF_D119

Table 61. Filter Bank B Memory Map

Page	PAGE_ID	Address	Register
7	0x07	0x00	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08	FIR_COEF_B000
7	0x07	0x0A	FIR_COEF_B001
7	0x07	0x0C to 0x7C	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E	FIR_COEF_B059
8	0x08	0x00	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08	FIR_COEF_B060
8	0x08	0x0A	FIR_COEF_B061
8	0x08	0x0C to 0x7C	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E	FIR_COEF_B119

Table 62. Filter Bank C Memory Map

Page	PAGE_ID	Address	Register
9	0x09	0x00	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08	FIR_COEF_C000
9	0x09	0x0A	FIR_COEF_C001
9	0x09	0x0C to 0x7C	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E	FIR_COEF_C059
10	0x0A	0x00	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08	FIR_COEF_C060
10	0x0A	0x0A	FIR_COEF_C061
10	0x0A	0x0C to 0x7C	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E	FIR_COEF_C119

Table 63. Filter Bank D Memory Map

Page	PAGE_ID	Address	Register
11	0x0B	0x00	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08	FIR_COEF_D000
11	0x0B	0x0A	FIR_COEF_D001
11	0x0B	0x0C to 0x7C	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E	FIR_COEF_D059
12	0x0C	0x00	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08	FIR_COEF_D060
12	0x0C	0x0A	FIR_COEF_D061
12	0x0C	0x0C to 0x7C	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory-programmed filter designs. They are all low-pass filters that have unity dc gain. Table 64 provides a summary of each filter design, and Figure 21 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 64. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	310
B	120	55
C	32	275
D	32	63

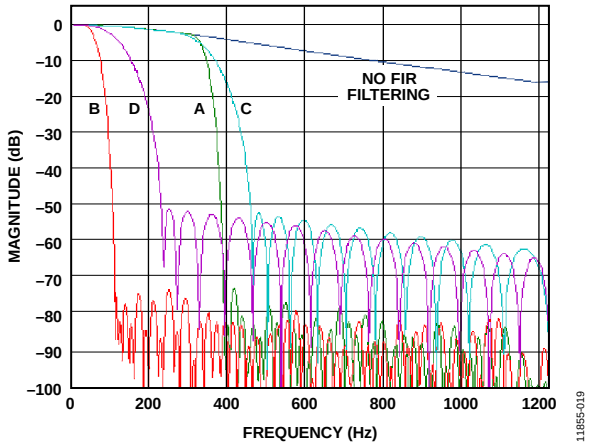

Figure 21. FIR Filter Frequency Response Curves

CALIBRATION

The ADIS16488A factory calibration produces correction formulas for the gyroscopes, accelerometers, magnetometers, and barometers, and then programs them into the flash memory. In addition, there are a series of user configurable calibration registers for in-system tuning.

GYROSCOPES

The user calibration for the gyroscopes includes registers for adjusting bias and sensitivity, as shown in Figure 22.

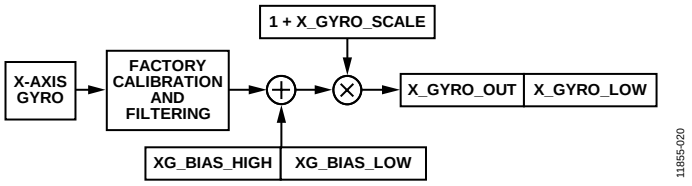

Figure 22. User Calibration Signal Path, Gyroscopes

Manual Bias Correction

The xG_BIAS_HIGH registers (see Table 65, Table 66, and Table 67) and xG_BIAS_LOW registers (see Table 68, Table 69, and Table 70) provide a bias adjustment function for the output of each gyroscope sensor.

Table 65. XG_BIAS_HIGH (Page 2, Base Address = 0x12)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, upper word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 66. YG_BIAS_HIGH (Page 2, Base Address = 0x16)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 67. ZG_BIAS_HIGH (Page 2, Base Address = 0x1A)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 68. XG_BIAS_LOW (Page 2, Base Address = 0x10)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 69. YG_BIAS_LOW (Page 2, Base Address = 0x14)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 70. ZG_BIAS_LOW (Page 2, Base Address = 0x18)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, lower word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Bias Null Command

The continuous bias estimator (CBE) accumulates and averages data in a 64-sample FIFO. The average time (t_A) for the bias estimates relies on the sample time base setting in NULL_CNFG[3:0] (see Table 71). Using the bias null command in GLOB_CMD[0] (see Table 115), load the correction factors of the CBE into the gyroscope offset correction registers (see Table 65, Table 66, Table 67, Table 68, Table 69, and Table 70). On/off controls for the sensors, provided by NULL_CNFG[13:8], update when issuing a bias null command. The factory default configuration for NULL_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and establishes the average time to ~26.64 seconds.

Table 71. NULL_CNFG (Page 3, Base Address = 0x0E)

Bits	Description (Default = 0x070A)
[15:14]	Not used
13	Z-axis acceleration bias correction enable (1 = enabled)
12	Y-axis acceleration bias correction enable (1 = enabled)
11	X-axis acceleration bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC), range: 0 to 13 (default = 10); $t_B = 2^{TBC}/2460$, time base $t_A = 64 \times t_B$, average time

Turn to Page 3 (DIN = 0x8003) and set GLOB_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the CBE. Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

Manual Sensitivity Correction

The x_GYRO_SCALE registers enable sensitivity adjustment (see Table 72, Table 73, and Table 74).

Table 72. X_GYRO_SCALE (Page 2, Base Address = 0x04)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 73. Y_GYRO_SCALE (Page 2, Base Address = 0x06)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 74. Z_GYRO_SCALE (Page 2, Base Address = 0x08)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Linear Acceleration on Effect on Gyroscope Bias

MEMS gyroscopes typically have a bias response to linear acceleration that is normal to their axis of rotation. The ADIS16488A offers an optional compensation function for this effect; the factory default setting (0x00C0) for the CONFIG register enables this function. To turn it off, turn to Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A40, DIN = 0x8B00). Note that this also keeps the point of percussion alignment function enabled.

Table 75. CONFIG (Page 3, Base Address = 0x0A)

Bits	Description (Default = 0x00C0)
[15:8]	Not used
7	Linear-*g* compensation for gyroscopes (1 = enabled)
6	Point of percussion alignment (1 = enabled)
[5:2]	Not used
1	Real-time clock, daylight savings time (1: enabled, 0: disabled)
0	Real-time clock control (1: relative/elapsed timer mode, 0: calendar mode)

ACCELEROMETERS

The user calibration for the accelerometers includes registers for adjusting bias and sensitivity, as shown in Figure 23.

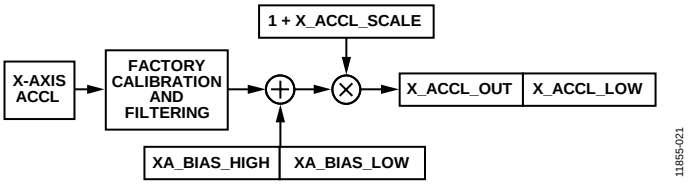

Figure 23. User Calibration Signal Path, Gyroscopes

Manual Bias Correction

The xA_BIAS_HIGH (see Table 76, Table 77, and Table 78) and xA_BIAS_LOW (see Table 79, Table 80, and Table 81) registers provide a bias adjustment function for the output of each accelerometer sensor. The xA_BIAS_HIGH registers use the same format as x_ACCL_OUT registers. The xA_BIAS_LOW registers use the same format as x_ACCL_LOW registers.

Table 76. XA_BIAS_HIGH (Page 2, Base Address = 0x1E)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 77. YA_BIAS_HIGH (Page 2, Base Address = 0x22)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 78. ZA_BIAS_HIGH (Page 2, Base Address = 0x26)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 79. XA_BIAS_LOW (Page 2, Base Address = 0x1C)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.0000122 m*g*

Table 80. YA_BIAS_LOW (Page 2, Base Address = 0x20)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, low word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.0000122 m*g*

Table 81. ZA_BIAS_LOW (Page 2, Base Address = 0x24)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, low word;, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g* ÷ 2^{16} = ~0.0000122 m*g*

Manual Sensitivity Correction

The x_ACCL_SCALE registers enable sensitivity adjustment (see Table 82, Table 83, Table 84).

Table 82. X_ACCL_SCALE (Page 2, Base Address = 0x0A)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 83. Y_ACCL_SCALE (Page 2, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 84. Z_ACCL_SCALE (Page 2, Base Address = 0x0E)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

MAGNETOMETERS

The user calibration registers enable both hard iron and soft iron correction, as shown in the following relationship:

$$\begin{bmatrix} M_{XC} \\ M_{YC} \\ M_{ZC} \end{bmatrix} = \begin{bmatrix} 1+S_{11} & S_{12} & S_{13} \\ S_{21} & 1+S_{22} & S_{23} \\ S_{31} & S_{32} & 1+S_{33} \end{bmatrix} \times \left(\begin{bmatrix} M_X \\ M_Y \\ M_Z \end{bmatrix} + \begin{bmatrix} H_X \\ H_Y \\ H_Z \end{bmatrix} \right)$$

where the M_X, M_Y, and M_Z variables represent the magnetometer data prior to application of the user correction formula, and the M_{XC}, M_{YC}, and M_{ZC} represent the magnetometer data after the application of the user correction formula.

Hard Iron Correction

Table 85, Table 86, and Table 87 describe the register format for the hard iron correction factors: H_X, H_Y, and H_Z. These registers use a twos complement format. Table 88 provides some numerical examples for converting the digital codes for these registers into their decimal equivalent.

Table 85. HARD_IRON_X (Page 2, Base Address = 0x28)

Bits	Description (Default = 0x0000)
[15:0]	X-axis magnetometer hard iron correction factor, H_X, twos complement, ±3.2767 gauss range, 0.1 mgauss/LSB, 0 gauss = 0x0000 (see Table 88)

Table 86. HARD_IRON_Y (Page 2, Base Address = 0x2A)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis magnetometer hard iron correction factor, H_Y, twos complement, ±3.2767 gauss range, 0.1 mgauss/LSB, 0 gauss = 0x0000 (see Table 88)

Table 87. HARD_IRON_Z (Page 2, Base Address = 0x2C)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis magnetometer hard iron correction factor, H_Z, twos complement, ±3.2767 gauss range, 0.1 mgauss/LSB, 0 gauss = 0x0000 (see Table 88)

Table 88. HARD_IRON_x Numerical Examples

Magnetic Field	Decimal	Hex	Binary
+3.2767 gauss	+32,767	0x7FFF	0111 1111 1111 1111
+0.2 mgauss	+2	0x0002	0000 0000 0000 0010
+0.1 mgauss	+1	0x0001	0000 0000 0000 0001
0 gauss	0	0x0000	0000 0000 0000 0000
−0.1 mgauss	−1	0xFFFF	1111 1111 1111 1111
−0.2 mgauss	−2	0xFFFE	1111 1111 1111 1110
−3.2768 gauss	−32,768	0x8000	1000 0000 0000 0000

Soft Iron Correction Matrix

The soft iron correction matrix contains correction factors for both sensitivity (S_{11}, S_{22}, S_{33}) and alignment (S_{12}, S_{13}, S_{21}, S_{23}, S_{31}, S_{32}). The registers that represent each soft iron correction factor are in Table 89 (S_{11}), Table 90 (S_{12}), Table 91 (S_{13}), Table 92 (S_{21}), Table 93 (S_{22}), Table 94 (S_{23}), Table 95 (S_{31}), Table 96 (S_{32}), and Table 97 (S_{33}). Table 98 offers some numerical examples for converting between the digital codes and their effect on the magnetometer output, in terms of percent change.

Table 89. SOFT_IRON_S11 (Page 2, Base Address = 0x2E)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{11}, twos complement format, see Table 98 for examples

Table 90. SOFT_IRON_S12 (Page 2, Base Address = 0x30)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{12}, twos complement format, see Table 98 for examples

Table 91. SOFT_IRON_S13 (Page 2, Base Address = 0x32)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{13}, twos complement format, see Table 98 for examples

Table 92. SOFT_IRON_S21 (Page 2, Base Address = 0x34)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{21}, twos complement format, see Table 98 for examples

Table 93. SOFT_IRON_S22 (Page 2, Base Address = 0x36)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{22}, twos complement format, see Table 98 for examples

Table 94. SOFT_IRON_S23 (Page 2, Base Address = 0x38)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{23}, twos complement format, see Table 98 for examples

Table 95. SOFT_IRON_S31 (Page 2, Base Address = 0x3A)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft-iron correction factor, S_{31}, twos complement format, see Table 98 for examples

Table 96. SOFT_IRON_S32 (Page 2, Base Address = 0x3C)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{32}, twos complement format, see Table 98 for examples

Table 97. SOFT_IRON_S33 (Page 2, Base Address = 0x3E)

Bits	Description (Default = 0x0000)
[15:0]	Magnetometer soft iron correction factor, S_{33}, twos complement format, see Table 98 for examples

Table 98. Soft Iron Correction, Numerical Examples

Delta (%)	Decimal	Hex	Binary
$+100 - 1/2^{16}$	+32,767	0x7FFF	0111 1111 1111 1111
$+200/2^{15}$	+2	0x0002	0000 0000 0000 0010
$+100/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-100/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-200/2^{15}$	−2	0xFFFE	1111 1111 1111 1110
−100	−32,768	0x8000	1000 0000 0000 0000

BAROMETERS

The BR_BIAS_HIGH register (see Table 99) and BR_BIAS_LOW register (Table 100) provide an offset control function and use the same format as the output registers, BAROM_OUT and BAROM_LOW.

Table 99. BR_BIAS_HIGH (Page 2, Base Address = 0x42)

Bits	Description (Default = 0x0000)
[15:0]	Barometric pressure bias correction factor, high word, twos complement, ±1.3 bar measurement range, 0 bar = 0x0000, 1 LSB = 40 µbar

Table 100. BR_BIAS_LOW (Page 2, Base Address = 0x40)

Bits	Description (Default = 0x0000)
[15:0]	Barometric pressure bias correction factor, low word, twos complement, ±1.3 bar measurement range, 0 bar = 0x0000, 1 LSB = 40 µbar ÷ 2^{16} = ~0.00061 µbar

RESTORING FACTORY CALIBRATION

Turn to Page 3 (DIN = 0x8003) and set GLOB_CMD[6] = 1 (DIN = 0x8240, DIN = 0x8300) to execute the factory calibration restore function. This function resets each user calibration register to 0, resets all sensor data to 0, and automatically updates the flash memory within 72 ms. See Table 115 for more information on GLOB_CMD.

POINT OF PERCUSSION ALIGNMENT

CONFIG[6] offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 24. To activate this feature, turn to Page 3 (DIN = 0x8003), then set CONFIG[6] = 1 (DIN = 0x8A40, DIN = 0x8B00). See Table 75 for more information on the CONFIG register.

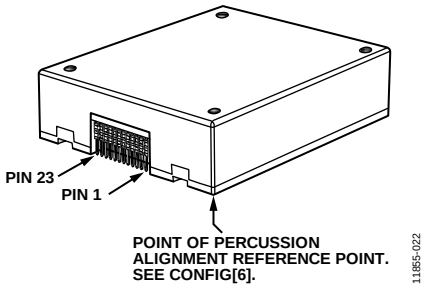

Figure 24. Point of Percussion Reference Point

ALARMS

Each sensor has an independent alarm function that provides controls for alarm magnitude, polarity, and enabling a dynamic rate-of-change option. The ALM_STS register (see Table 50) contains the alarm output flags and the FNCTIO_CTRL register (see Table 118) provides an option for configuring one of the digital input/output lines as an alarm indicator.

STATIC ALARM USE

The static alarm setting compares the output of each sensor with the trigger settings in the xx_ALM_MAGN registers (see Table 101 through Table 110) of that sensor.

Table 101. XG_ALM_MAGN (Page 3, Base Address = 0x28)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 102. YG_ALM_MAGN (Page 3, Base Address = 0x2A)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 103. ZG_ALM_MAGN (Page 3, Base Address = 0x2C)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 104. XA_ALM_MAGN (Page 3, Base Address = 0x2E)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 105. YA_ALM_MAGN (Page 3, Base Address = 0x30)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 106. ZA_ALM_MAGN (Page 3, Base Address = 0x32)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

Table 107. XM_ALM_MAGN (Page 3, Base Address = 0x34)

Bits	Description (Default = 0x0000)
[15:0]	X-axis magnetometer alarm threshold settings, twos complement, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 108. YM_ALM_MAGN (Page 3, Base Address = 0x36)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis magnetometer alarm threshold settings, twos complement, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 109. ZM_ALM_MAGN (Page 3, Base Address = 0x38)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis magnetometer alarm threshold settings, twos complement, 0 gauss = 0x0000, 1 LSB = 0.1 mgauss

Table 110. BR_ALM_MAGN (Page 3, Base Address = 0x3A)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis barometer alarm threshold settings, twos complement, 0 bar = 0x0000, 1 LSB = 40 µbar

Static Alarm Polarity Controls

The alarm polarity settings, located in the ALM_CNFG_x registers (see Table 111 to Table 113), establish the relationship for the condition that causes the corresponding alarm flag to be active. For example, when ALM_CNFG_0[13] = 1, the alarm flag for the x-axis accelerometer (ALM_STS[3], see Table 50) becomes active (equal to 1) when X_ACCL_OUT is greater than XA_ALM_MAGN.

Table 111. ALM_CNFG_0 (Page 3, Base Address = 0x20)

Bits	Description (Default = 0x0000)
15	X-axis accelerometer alarm (1 = enabled)
14	Not used
13	X-axis accelerometer alarm polarity (1 = greater than)
12	X-axis accelerometer dynamic enable (1 = enabled)
11	Z-axis gyroscope alarm (1 = enabled)
10	Not used
9	Z-axis gyroscope alarm polarity (1 = greater than)
8	Z-axis gyroscope dynamic enable (1 = enabled)
7	Y-axis gyroscope alarm (1 = enabled)
6	Not used
5	Y-axis gyroscope alarm polarity (1 = greater than)
4	Y-axis gyroscope dynamic enable (1 = enabled)
3	X-axis gyroscope alarm (1 = enabled)
2	Not used
1	X-axis gyroscope alarm polarity (1 = greater than)
0	X-axis gyroscope dynamic enable (1 = enabled)

Table 112. ALM_CNFG_1 (Page 3, Base Address = 0x22)

Bits	Description (Default = 0x0000)
15	Y-axis magnetometer alarm (1 = enabled)
14	Not used
13	Y-axis magnetometer alarm polarity (1 = greater than)
12	Y-axis magnetometer dynamic enable (1 = enabled)
11	X-axis magnetometer (1 = enabled)
10	Not used
9	X-axis magnetometer alarm polarity (1 = greater than)
8	X-axis magnetometer dynamic enable (1 = enabled)
7	Z-axis accelerometer alarm (1 = enabled)
6	Not used
5	Z-axis accelerometer alarm polarity (1 = greater than)
4	Z-axis accelerometer dynamic enable (1 = enabled)
3	Y-axis accelerometer alarm (1 = enabled)
2	Not used
1	Y-axis accelerometer alarm polarity (1 = greater than)
0	Y-axis accelerometer dynamic enable (1 = enabled)

Table 113. ALM_CNFG_2 (Page 3, Base Address = 0x24)

Bits	Description (Default = 0x0000)
[15:8]	Not used
7	Barometer alarm (1 = enabled)
6	Not used
5	Barometer alarm polarity (1 = greater than)
4	Barometer dynamic enable (1 = enabled)
3	Z-axis magnetometer alarm (1 = enabled)
2	Not used
1	Z-axis magnetometer alarm polarity (1 = greater than)
0	Z-axis magnetometer dynamic enable (1 = enabled)

DYNAMIC ALARM USE

The dynamic alarm setting provides the option to compare the change in the output of each sensor over a period of 48.7 ms with that sensor's xx_ALM_MAGN register.

Alarm Example

Table 114 offers an alarm configuration example, which sets the z-axis gyroscope alarm to trip when Z_GYRO_OUT > 131.1°/sec (0x199B).

Table 114. Alarm Configuration Example

DIN	Description
0xAC9B	Set ZG_ALM_MAGN[7:0] = 0x9B
0xAD19	Set ZG_ALM_MAGN[15:8] = 0x19
0xA000	Set ALM_CNFG_0[7:0] = 0x00
0xA103	Set ALM_CNFG_0[15:8] = 0x03

SYSTEM CONTROLS

The ADIS16488A provides a number of system level controls for managing its operation, which include reset, self test, calibration, memory management, and input/output configuration.

GLOBAL COMMANDS

The GLOB_CMD register (see Table 115) provides trigger bits for several operations. Write 1 to the appropriate bit in GLOB_CMD to start a function. After the function completes, the bit restores to 0.

Table 115. GLOB_CMD (Page 3, Base Address = 0x02)

Bits	Description	Execution Time
[15:8]	Not used	Not applicable
7	Software reset	120 ms
6	Factory calibration restore	75 ms
[5:4]	Not used	Not applicable
3	Flash memory update	375 ms
2	Flash memory test	50 ms
1	Self test	12 ms
0	Bias null	See Table 71

Software Reset

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[7] = 1 (DIN = 0x8280, DIN = 0x8300) to reset the operation, which removes all data, initializes all registers from their flash settings, and starts data collection. This function provides a firmware alternative to the $\overline{\text{RST}}$ pin (see Table 6, Pin 8).

Automatic Self-Test

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[1] = 1 (DIN = 0x8202, then DIN = 0x8300) to run an automatic self test routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate the self test on each sensor.
3. Measure the output on each sensor.
4. Deactivate the self test on each sensor.
5. Calculate the difference with self test on and off.
6. Compare the difference with internal pass/fail criteria.
7. Report the pass/fail results for each sensor in DIAG_STS.

After waiting 12 ms for this test to complete, turn to Page 0 (DIN = 0x8000) and read DIAG_STS using DIN = 0x0A00. Using an external clock can extend this time. When using an external clock of 100 Hz, this time extends to 35 ms. Note that 100 Hz is too slow for optimal sensor performance.

MEMORY MANAGEMENT

The data retention of the flash memory depends on temperature and the number of write cycles. Figure 25 characterizes the dependence on temperature, and the FLSHCNT_LOW and FLSHCNT_HIGH registers (see Table 116 and Table 117) provide a running count of flash write cycles. The flash updates every time GLOB_CMD[6], GLOB_CMD[3], or GLOB_CMD[0] is set to 1.

Table 116. FLSHCNT_LOW (Page 2, Base Address = 0x7C)

Bits	Description
[15:0]	Binary counter; number of flash updates, lower word

Table 117. FLSHCNT_HIGH (Page 2, Base Address = 0x7E)

Bits	Description
[15:0]	Binary counter; number of flash updates, upper word

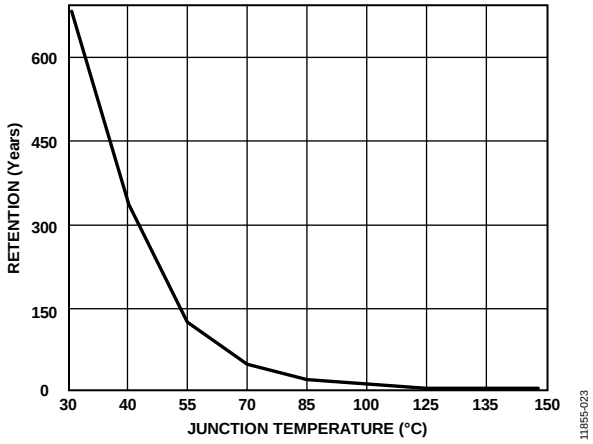

Figure 25. Flash Memory Retention

Flash Memory Test

Turn to Page 3 (DIN = 0x8003), and then set GLOB_CMD[2] = 1 (DIN = 0x8204, DIN = 0x8300) to run a checksum test of the internal flash memory, which compares a factory programmed value with the current sum of the same memory locations. The result of this test loads into SYS_E_FLAG[6]. Turn to Page 0 (DIN = 0x8000) and use DIN = 0x0800 to read SYS_E_FLAG.

GENERAL-PURPOSE INPUT/OUTPUT

There are four general-purpose input/output pins: DIO1, DIO2, DIO3, and DIO4. The FNCTIO_CTRL register controls the basic function of each input/output pin, which provides a number of useful functions. Each input/output pin only supports one function at a time. In cases where a single pin has two different assignments, the enable bit for the lower priority function automatically resets to zero and is disabled. The priority is (1) data ready, (2) sync clock input, (3) alarm indicator, and (4) general purpose, where 1 identifies the highest priority and 4 indicates the lowest priority.

Table 118. FNCTIO_CTRL (Page 3, Base Address = 0x06)

Bits	Description (Default = 0x000D)
[15:12]	Not used
11	Alarm indicator: 1 = enabled, 0 = disabled
10	Alarm indicator polarity: 1 = positive, 0 = negative
[9:8]	Alarm indicator line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
7	Sync clock input enable: 1 = enabled, 0 = disabled
6	Sync clock input polarity: 1 = rising edge, 0 = falling edge
[5:4]	Sync clock input line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
3	Data-ready enable: 1 = enabled, 0 = disabled
2	Data ready polarity: 1 = positive, 0 = negative
[1:0]	Data ready line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4

Data-Ready Indicator

FNCTIO_CTRL[3:0] provide some configuration options for using one of the DIOx lines as a data ready indicator signal, which can drive the interrupt control line of a processor. The factory default assigns DIO2 as a positive polarity, data ready signal. Use the following sequence to change this assignment to DIO1 with a negative polarity: turn to Page 3 (DIN = 0x8003) and set FNCTIO_CTRL[3:0] = 1000 (DIN = 0x8608, then DIN = 0x8700). The timing jitter on the data ready signal is ±1.4 µs.

Input Sync/Clock Control

FNCTIO_CTRL[7:4] provide some configuration options for using one of the DIOx lines as an input synchronization signal for sampling inertial sensor data. For example, use the following sequence to establish DIO4 as a positive polarity, input clock pin and keep the factory default setting for the data ready function: turn to Page 3 (DIN = 0x8003) and set FNCTIO_CTRL[7:0] = 0xFD (DIN = 0x86FD, then DIN = 0x8700). Note that this command also disables the internal sampling clock, and no data sampling occurs without the input clock signal. When selecting a clock input frequency, consider the 330 Hz sensor bandwidth because undersampling the sensors can degrade noise and stability performance.

General-Purpose Input/Output Control

When FNCTIO_CTRL does not configure a DIOx pin, GPIO_CTRL provides register controls for general-purpose use of the pin. GPIO_CTRL[3:0] provides input/output assignment controls for each line. When the DIOx lines are inputs, monitor their level by reading GPIO_CTRL[7:4]. When the DIOx lines are used as outputs, set their level by writing to GPIO_CTRL[7:4].

For example, use the following sequence to set DIO1 and DIO3 as high and low output lines, respectively, and set DIO2 and DIO4 as input lines. Turn to Page 3 (DIN = 0x8003) and set GPIO_CTRL[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

Table 119. GPIO_CTRL (Page 3, Base Address = 0x08)

Bits	Description (Default = 0x00X0)[1]
[15:8]	Don't care
7	General-Purpose input/output Line 4 (DIO4) data level
6	General-Purpose input/output Line 3 (DIO3) data level
5	General-Purpose input/output Line 2 (DIO2) data level
4	General-Purpose input/output Line 1 (DIO1) data level
3	General-Purpose input/output Line 4 (DIO4) direction control (1 = output, 0 = input)
2	General-Purpose input/output Line 3 (DIO3) direction control (1 = output, 0 = input)
1	General-Purpose input/output Line 2 (DIO2) direction control (1 = output, 0 = input)
0	General-Purpose input/output Line 1 (DIO1) direction control (1 = output, 0 = input)

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

POWER MANAGEMENT

The SLP_CNT register (see Table 120) provides controls for both power-down mode and sleep modes. The trade-off between power-down mode and sleep mode is between idle power and recovery time. Power-down mode offers the best idle power consumption but requires the most time to recover. In addition, all volatile settings are lost during power-down but are preserved during sleep mode.

For timed sleep mode, turn to Page 3 (DIN = 0x8003), write the amount of sleep time to SLP_CNT[7:0] and then, set SLP_CNT[8] = 1 (DIN = 0x9101) to start the sleep period.

For a timed power-down period, change the last command to set SLP_CNT[9] = 1 (DIN = 0x9102).

To power down or sleep for an indefinite period, set SLP_CNT[7:0] = 0x00 first, then set either SLP_CNT[8] or SLP_CNT[9] to 1. Note that the command takes effect when the $\overline{CS}$ line goes high.

To awaken the device from sleep or power-down mode, use one of the following options to restore normal operation:

- Assert $\overline{CS}$ from high to low.
- Pulse $\overline{RST}$ low, then high again.
- Cycle the power.

For example, set SLP_CNT[7:0] = 0x64 (DIN = 0x9064), then set SLP_CNT[8] = 1 (DIN = 0x9101) to start a sleep period of 100 seconds. If the sleep mode and power-down mode bits are both set high, the normal sleep mode bit (SLP_CNT[8]) takes precedence.

Table 120. SLP_CNT (Page 3, Base Address = 0x10)

Bits	Description
[15:10]	Not used
9	Power-down mode
8	Normal sleep mode
[7:0]	Programmable time bits; 1 sec/LSB; 0x00 = indefinite

General-Purpose Registers

The USER_SCR_x registers (see Table 121, Table 122, Table 123, and Table 124) provide four 16-bit registers for storing data.

Table 121. USER_SCR_1 (Page 2, Base Address = 0x74)

Bits	Description
[15:0]	User defined

Table 122. USER_SCR_2 (Page 2, Base Address = 0x76)

Bits	Description
[15:0]	User defined

Table 123. USER_SCR_3 (Page 2, Base Address = 0x78)

Bits	Description
[15:0]	User defined

Table 124. USER_SCR_4 (Page 2, Base Address = 0x7A)

Bits	Description
[15:0]	User defined

Real-Time Clock Configuration/Data

The VDDRTC power supply pin (see Table 6, Pin 23) provides a separate supply for the real-time clock (RTC) function. This enables the RTC to keep track of time, even when the main supply (VDD) is off.

Configure the RTC function by selecting one of two modes in CONFIG[0] (see Table 75). The real-time clock data is available in the TIME_MS_OUT register (see Table 125), TIME_DH_OUT register (see Table 126), and TIME_YM_OUT register (see Table 127). When using the elapsed timer mode, the time data registers start at 0x0000 when the device starts up (or resets) and begin keeping time in a manner that is similar to a stopwatch.

When using the clock/calendar mode, write the current time to the real-time registers in the following sequence: seconds (TIME_ MS_OUT[5:0]), minutes (TIME_ MS_OUT[13:8]), hours (TIME_DH_OUT[5:0]), day (TIME_DH_OUT[12:8]), month (TIME_YM_OUT[3:0]), and year (TIME_YM_OUT[14:8]). The updates to the timer only become active after a write is completed correctly to the TIME_YM_OUT[14:8] byte.

The real-time clock registers reflect the newly updated values only after the next seconds tick of the clock that follows the write to TIME_YM_OUT[14:8] (year). Writing to TIME_YM_OUT[14:8] activates all timing values; therefore, always write to this location last when updating the timer, even if the year information does not require updating.

Write the current time to each time data register after setting CONFIG[0] = 1 (DIN = 0x8003, DIN = 0x8A01). Note that CONFIG[1] provides a bit for managing daylight savings time. After the CONFIG and TIME_xx_OUT registers are configured, set GLOB_CMD[3] = 1 (DIN = 0x8003, DIN = 0x8204, DIN = 0x8300) to back up these settings in flash, and use a separate 3.3 V source to supply power to the VDDRTC function. Note that access to time data in the TIME_xx_OUT registers requires normal operation (VDD = 3.3 V and full startup), but the timer function only requires that VDDRTC = 3.3 V when the remainder of the ADIS16488A is turned off.

Table 125. TIME_MS_OUT (Page 0, Base Address = 0x78)

Bits	Description
[15:14]	Not used
[13:8]	Minutes, binary data, range = 0 to 59
[7:6]	Not used
[5:0]	Seconds, binary data, range = 0 to 59

Table 126. TIME_DH_OUT (Page 0, Base Address = 0x7A)

Bits	Description
[15:13]	Not used
[12:8]	Day, binary data, range = 1 to 31
[7:6]	Not used
[5:0]	Hours, binary data, range = 0 to 23

Table 127. TIME_YM_OUT (Page 0, Base Address = 0x7C)

Bits	Description
[15]	Not used
[14:8]	Year, binary data, range = 0 to 99, relative to 2000 A.D.
[7:4]	Not used
[3:0]	Month, binary data, range = 1 to 12

APPLICATIONS INFORMATION

MOUNTING BEST PRACTICES

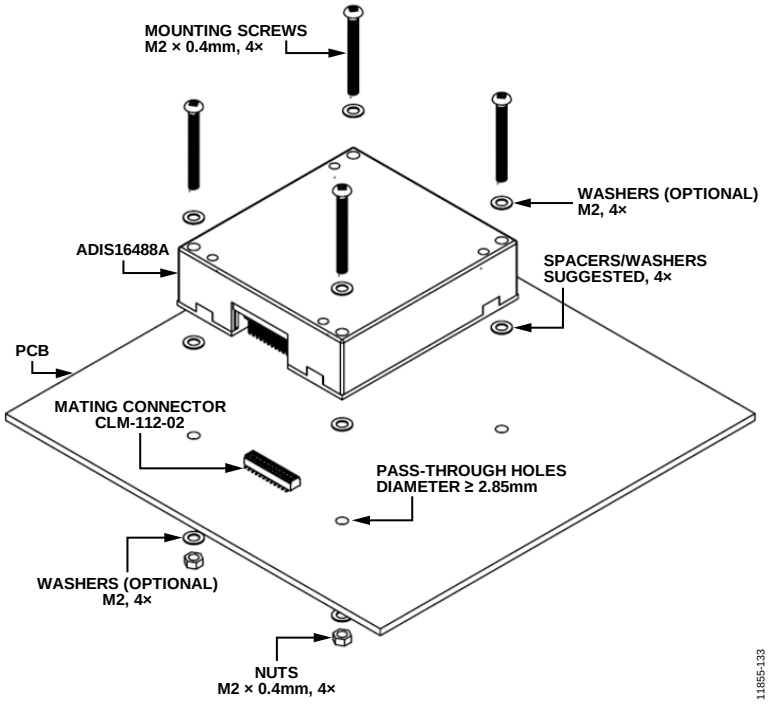

Figure 26. Mounting Example

For best performance, follow these simple rules when installing the ADIS16488A into a system:

1. Eliminate opportunity for translational force (x- and y-axis direction, per Figure 6) application on the electrical connector.
2. Isolate mounting force to the four corners, on the portion of the package surface that surrounds the mounting holes.
3. Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch-ounces (0.285 N-m).

These three rules help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 26 provides an example that leverages washers to set the package off the mounting surface and uses 2.85 mm pass-through holes and backside washers/nuts for attachment. Figure 27 and Figure 28 provide some details for mounting hole and connector alignment pin drill locations.

For more information on mounting the ADIS16488A, see the AN-1295 Application Note.

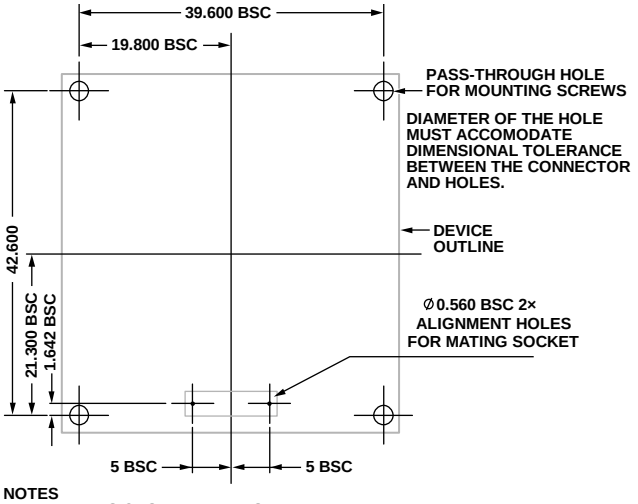

Figure 27. Suggested PCB Layout Pattern, Connector Down

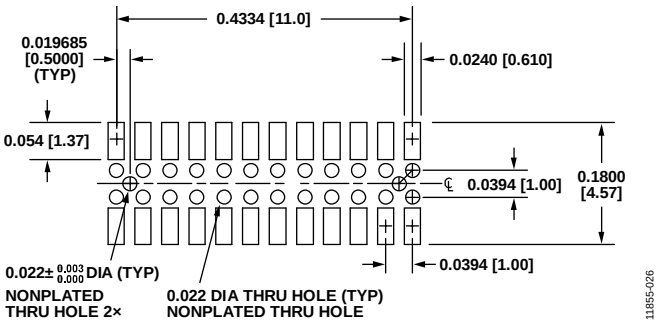

Figure 28. Suggested Layout and Mechanical Design When Using Samtec P/N CLM-112-02-G-D-A for the Mating Connector

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16488A, which means that it provides access to the ADIS16488A through larger connectors that support standard 1 mm ribbon cabling. It also provides four mounting holes for attachment of the ADIS16488A to the breakout board.

PC-Based Evaluation, EVAL-ADIS2

Use the EVAL-ADIS2 and the ADIS16IMU1/PCBZ to evaluate the ADIS16488A on a PC-based platform.

POWER SUPPLY CONSIDERATIONS

The ADIS16488A has approximately 24 µF of capacitance across the VDD and GND pins. Whereas this capacitor bank provides a large amount of localized filtering, it also presents an opportunity for excessive charging current when the VDD voltage ramps too quickly. Use the following relationship to help determine the appropriate VDD voltage profile, with respect to any current-limit functions that can cause the power supply to lose regulation and potentially introduce unsafe conditions for the ADIS16488A.

$$i(t) = C\,dV/dt$$

In addition to managing the initial voltage ramp, take note of the transient current demand that the ADIS16488A requires during its start-up/self initialization process. When VDD reaches 2.85 V, the ADIS16488A begins its start-up process. Figure 29 offers a broad perspective that shows when to expect the spikes in current, whereas Figure 30 provides more detail on the current/time behavior during the peak transient condition, which typically occurs approximately 350 ms after VDD reaches 2.85 V.

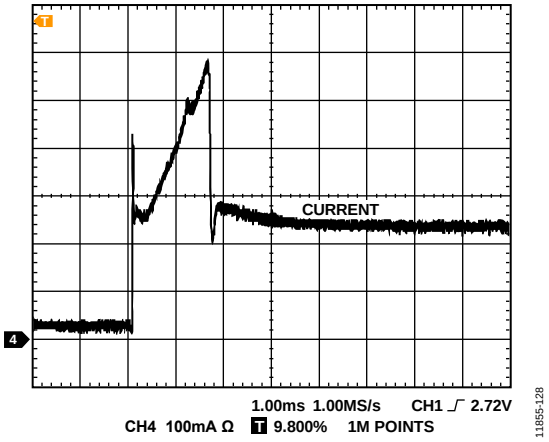

Figure 29. Transient Current Demand, Start Up

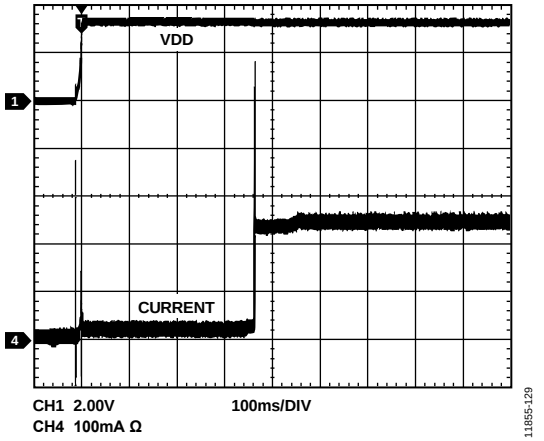

Figure 30. Transient Current Demand, Peak Demand

X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, can affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16488A to this type of inspection.

OUTLINE DIMENSIONS

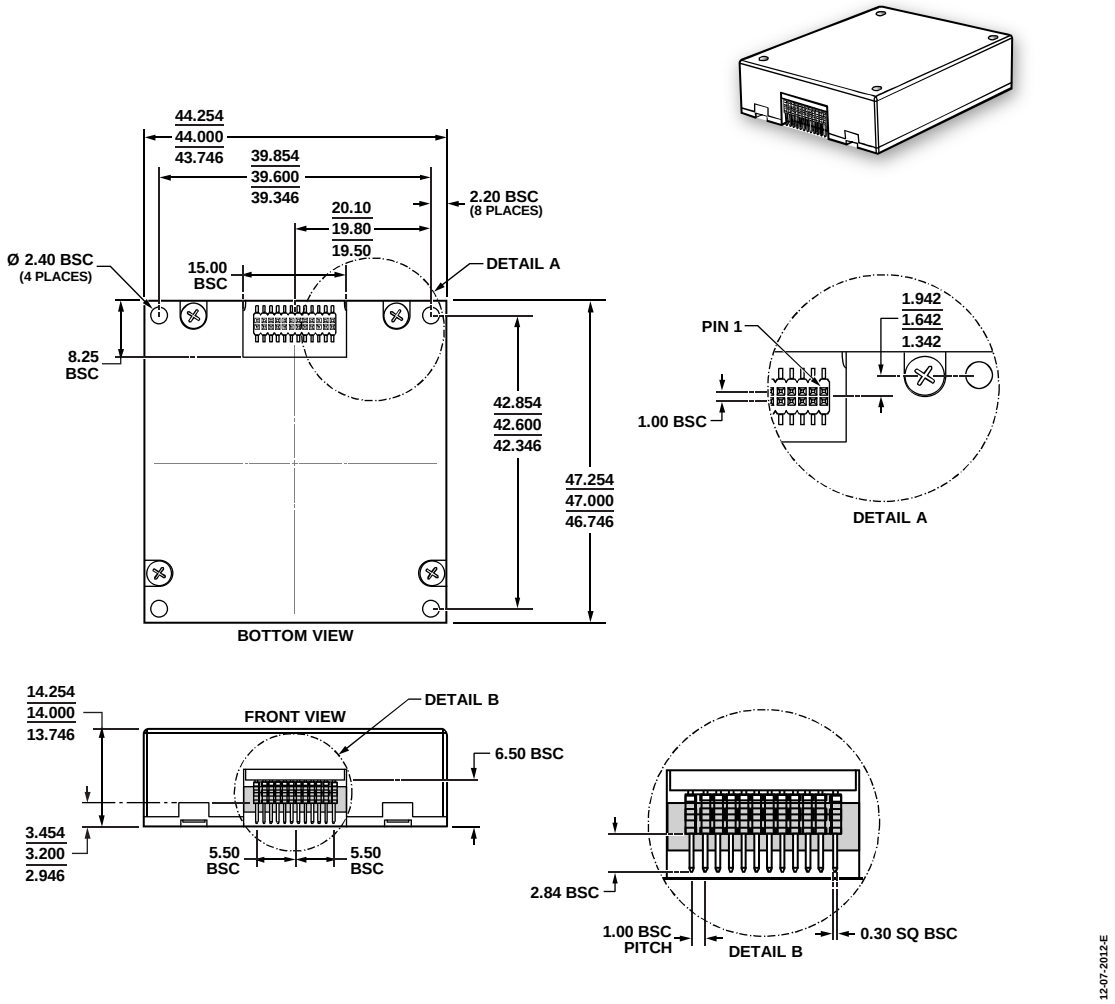

Figure 31. 24-Lead Module with Connector Interface [MODULE]
(ML-24-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16488BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface [MODULE]	ML-24-6
ADIS16488CMLZ	−55°C to +105°C	24-Lead Module with Connector Interface [MODULE]	ML-24-6

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

ADIS16488BMLZ ADIS16488CMLZ